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Question Paper Code : 51446

B.E. /B. Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Third Semester

Electronics and Communication Engineering

EC 2205/EC 36/080290011 – ELECTRONIC CIRCUITS – I

(Common to Medical Electronics Engineering)

(Regulations 2008)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. List out the advantages of self bias over other BJT biasing methods.
2. Draw the DC load line of the circuit shown in Figure-2.

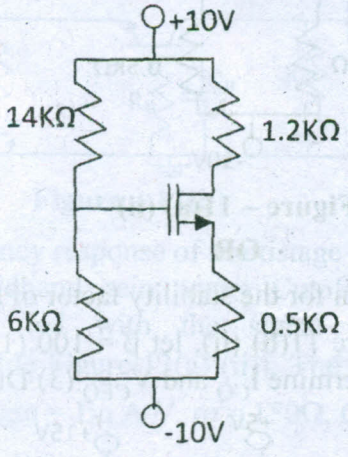

Figure-2

3. Define Miller's theorem.
4. Define CMRR. How to improve CMRR ?
5. Differentiate between Class A and Class S amplifier.
6. Define cross-over distortion. How to overcome cross-over distortion ?
7. Determine f_{3B} of the short-circuit current gain of BJT, rbe = 2.6kΩ, Cbe = 2pF and Cb c= 0.1pF
8. Differentiate between half-wave-rectifier and full-wave-rectifier.
9. Define gain-bandwidth product.
10. Compare between LC and π filter.

PART – B (5 × 16 = 80 Marks)

11. (a) (i) Determine the quiescent current and voltage values in a p-channel JFET circuit. **(6)**

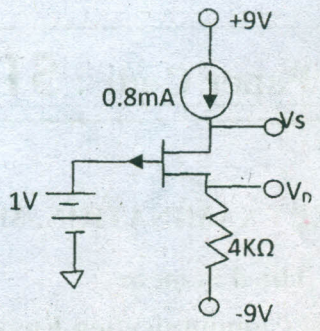

Figure – 11(a) (i)

(ii) For the MOSFET transistor in the circuit in Figure 11(a) (ii), the parameters are Vtn = 2V, kn' = 60μA/V^2 and W/L=60. (1) Determine V_{GS},I_D and V_{DS}. (2) Draw the DC load line. **(10)**

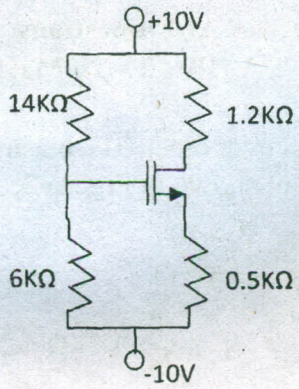

Figure – 11(a) (ii)

OR

(b) (i) Derive an expression for the stability factor of a self-bias circuit. **(6)**

(ii) The circuit in Figure 11(b) (ii), let β = 100 (1) Find V_{TH} and R_{TH} for the base circuit (2) Determine I_{CQ} and V_{CEQ} (3) Draw the DC load line. **(10)**

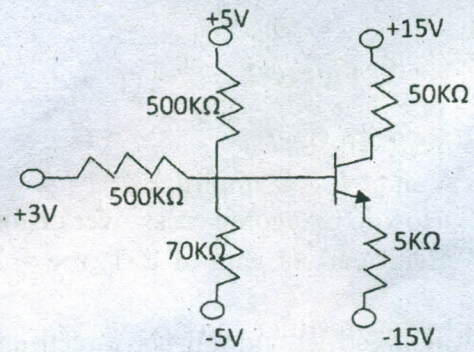

Figure 11(b) (ii)

12. (a) (i) For each transistor in the Darlington circuit shown in Figure 12(a) (i) has the parameters of $\beta = 100$, $V_A = \infty$. Determine its overall voltage gain, input impedance and output impedance. **(8)**

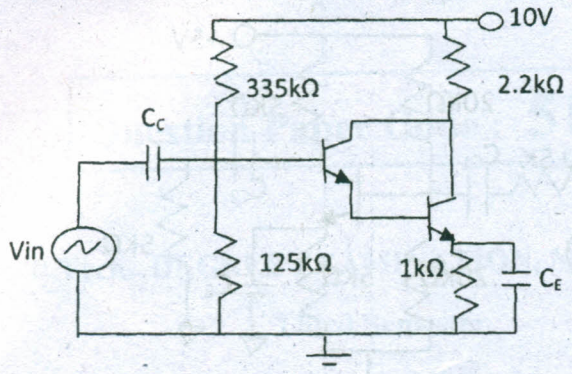

Figure – 12(a) (i)

(ii) Determine the small signal voltage gain, input impedance and output impedance of common source FET amplifier. **(8)**

OR

(b) For the circuit in Figure 12(b), the parameters are $R_B = 100$ kΩ, $R_E = 10$ kΩ, $R_C = 10$ kΩ, $V_{CC} = V_{EE} = 10$ V, $R_L = 1$ kΩ, $R_S = 1$ kΩ, $\beta = 125$ and $V_A = \infty$. (1) Determine the small signal voltage gain (2) Determine small signal current gain (3) Determine the input resistance, fin (4) Determine the output resistance, R_o. **(16)**

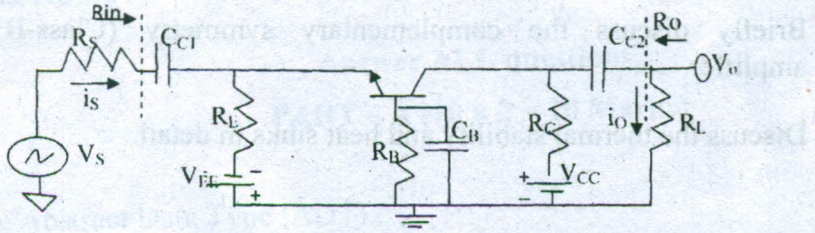

Figure – 12(b)

13. (a) (i) Discuss the frequency response of multistage amplifier in detail. **(8)**

(ii) Determine the midband gain, upper Cutoff frequency of a Common-Source amplifier fed with the signal having internal resistance Rsig = 100 kΩ (vide Figure 13(a) (ii)). The amplifier has $R_G = 4.7$ MΩ, $R_D = R_L = 15$ kΩ, gm = 1m A/V, ro = 150Ω, Cgs = 1pF and Cgd = 0.4 pF. **(8)**

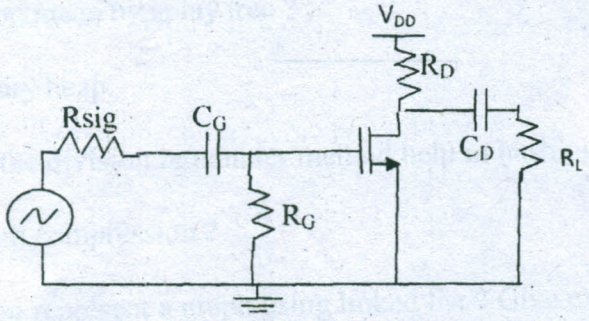

Figure – 13(a) (ii)

OR

(b) Determine the mid-band gain and bandwidth of a CE amplifier (vide Figure 13(b)). Assume lower cutoff frequency is 100 Hz, (ii) Find C_{C1}, C_{C2} and C_E. Let $\beta = 100$, cbe = 4pF, cbc=0.2pF and $V_A = \infty$. (16)

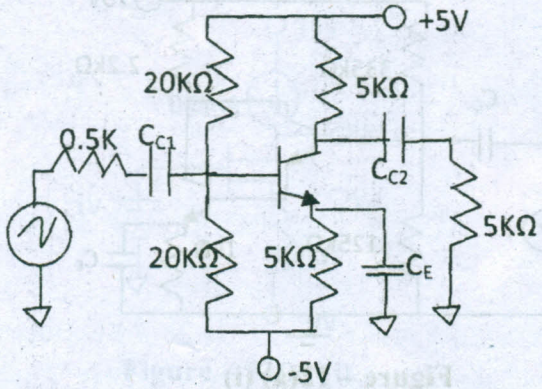

Figure – 13(b)

14. (a) (i) Explain the second-order harmonic distortion in detail. (8)

(ii) Explain the Class D amplifier in detail. (8)

OR

(b) (i) Briefly discuss the complementary symmetry (Class-B) push-pull amplifier. (8)

(ii) Discuss the thermal stability and heat sinks in detail. (8)

15. (a) Explain the Switched-Mode power supply design in detail. (16)

OR

(b) (i) Explain the AC power control using SCR in detail. (8)

(ii) Explain the performances measures of rectifiers in detail. (8)
