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Question Paper Code : 31399

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Fourth Semester

Electrical and Electronics Engineering

EE 2255/EE 46/EC 1261 A/10133 EE 406 A/080280029 — DIGITAL LOGIC CIRCUITS

(Regulation 2008/2010)

(Common to PTEE 2255 – Digital Logic Circuits for B.E. (Part-Time) Third Semester Electrical and Electronics Engineering – Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. What is meant by non weighted codes?

2. List the names of universal gates.

3. Differentiate sequential circuits and combinational circuits.

4. What is meant by state assignment?

5. What is meant by transition table?

6. Name the types of hazards.

7. What are the different classifications of memory?

8. Draw 4×2 ROM with AND-OR gates.

9. What is the function of wait statement in VHDL package?

10. Write the explanation of T'Base and T'Low predefined attributes.

PART B — ($5 \times 16 = 80$ marks)

11. (a) (i) Express the function $F = A + \overline{B}C$ in

(1) Canonical SOP form and

(2) Canonical POS form. (8)

(ii) Design BCD to Excess 3 code converter. (8)

Or

(b) (i) Simplify using K-map

$$F(A,B,C,D) = \sum m(7,8,9) + d(10,11,12,13,14,15)$$ (8)

(ii) Design a full subtractor using half subtractors. (8)

12. (a) A sequential circuit has two JK flip flops A and B. The flip flop input functions are :

$J_A = B \quad J_B = \overline{x}$

$K_A = B\overline{x} \quad K_B = A \oplus x$

(i) Draw the logic diagram of the circuit (5)

(ii) Tabulate the state table (6)

(iii) Draw the state diagram. (5)

Or

(b) Using JK flip flops, design a synchronous counter which counts in the sequence 000, 001, 010, 011, 100, 101, 110, 111, 000.

13. (a) Derive the transition table and primitive flow table for the functional mode asynchronous sequential circuit shown in fig.13(a).

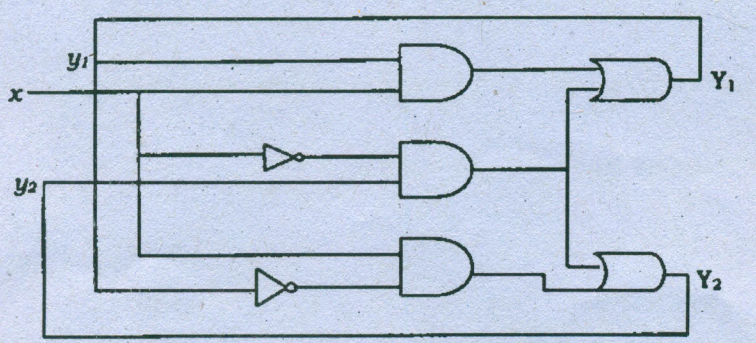

Fig. 13(a)

Or

(b) Design a pulse mode asynchronous sequential circuit, that has two inputs X_1 and X_2, one Mealy output Z_1 and one Moore output Z_2. The Mealy output is coincident with the third consecutive pulse on input X_2 and the Moore output occurs after the third consecutive pulse on input X_2 or after any pulse that occurs on input X_1.

14. (a) (i) Implement a 1M × 4 RAM using 512K × 4 RAM. (8)

(ii) Explain in details about TTL with open Collector output configuration. (8)

Or

(b) (i) Implement the following functions using PLA

$F_1 = \sum m(1,2,4,6)$; $F_2 = \sum m(0,1,6,7)$; $F_3 = \sum m(2,6)$. (8)

(ii) Demonstrate the CMOS logic circuit configuration and characteristics in details. (8)

15. (a) Explain the structural VHDL description for a 2 to 4 decoder in details.

Or

(b) Write a VHDL program and explain the design procedure of 8 bit comparator.