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Question Paper Code : 97064

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Third Semester

Electrical and Electronics Engineering

EE 6301 — DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering and Instrumentation and Control Engineering)

(Regulation 2013)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Determine $(377)_{10}$ in Octal and Hexa-Decimal equivalent.

2. Compare the totem-pole output with open-collector output?

3. Given $F = B' + A'B + A'C'$: Identify the redundant term using K-Map.

4. Give one application each for Multiplexer and Decoder.

5. Show how the JK flip flop can be modified into a D flip flop or a T flipflop.

6. Differentiate between Mealy and Moore models.

7. What is a deadlock condition?

8. Draw the block diagram of PLA.

9. Write a VHDL code for 2×1 MUX.

10. State the advantage of package declaration over component declaration.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Given that a frame with bit sequence 1101011011 is transmitted, it has been received as 1101011010. Determine the method of detecting the error using any one error detecting code. (8)

    (ii) Draw the MOS logic circuit for NOT gate and explain its operation. (8)

Or

    (b) (i) Explain Hamming code with an example. State its advantages over parity codes. (8)

    (ii) Design a TTL logic circuit for a 3-input NAND gate. (8)

12. (a) (i) Minimize the function $F(a, b, c, d) = \Sigma(0, 4, 6, 8, 9, 10, 12)$ with $d = \Sigma(2, 13)$. Implement the function using only NOR gates. (8)

    (ii) Design a Full Subtractor and implement it using logic gates. (8)

Or

    (b) (i) Implement the function $F(p, q, r, s) = \Sigma(0, 1, 2, 4, 7, 10, 11, 12)$ using Decoder. (8)

    (ii) Design a 4-bit Binary to gray code converter and implement it using logic gates. (8)

13. (a) (i) Design an asynchronous Modulo-8 Down counter using JK flipflops. (8)

    (ii) Explain the circuit of a SR flip-flop and explain its operation. (8)

Or

    (b) (i) Design synchronous sequential circuit that goes through the count sequence 1,3,4,5 repeatedly. Use T flip-flops for your design. (8)

    (ii) Explain the various types of triggering with suitable diagrams. Compare their merits and demerits. (8)

14. (a) Explain the various types of hazards in sequential circuit design and the methods to eliminate them. Give suitable examples. (16)

Or

    (b) Describe with reasons, the effect of races in asynchronous sequential circuit design. Explain its types with illustrations. Show the method of race-free state assignments with examples. (16)

15. (a) (i) Explain the digital system design flow sequence with the help of a flow chart. (8)

    (ii) Write a VHDL code for a 4-bit universal shift register. (8)

Or

(b) Explain the concept of Behavioural modeling and Structural modeling in VHDL. Take the example of Full Adder design for both and write the coding. (16)

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