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Question Paper Code : 80366

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Third Semester

Electrical and Electronics Engineering

EE 6301 — DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering and Instrumentation and Control Engineering)

(Regulations 2013)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Construct OR gate and AND gate using NAND gates.

2. Convert the following Excess - 3 numbers into decimal numbers.
   (a)   1011
   (b)   1001 0011 0111

3. Convert the given expression in canonical SOP form
   $Y = AB + A'C + BC'$

4. Draw the truth table of 2 :1 MUX.

5. Differentiate Mealy and Moore model.

6. Draw the state diagram of JK flip flop.

7. What is static hazard and dynamic hazard?

8. Define races in asynchronous sequential circuits.

9. Write VHDL behavioral model for D flip flop.

10. Write the VHDL code for a logical gate which gives high output only when both the inputs are high.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Explain with an aid of circuit diagram the operation of 2 input CMOS NAND gate and list out its advantages over other logic families.   (10)

    (ii) Given the two binary numbers $X = 1010100$ and $Y = 1000011$, perform the subtraction $Y - X$ by using 2's complements.   (3)

Or

    (b) (i) Explain in detail the usage of Hamming codes for error detection and error correction with an example considering the data bits as 0101.   (10)

    (ii) Convert 23.625_{10} to octal (base 8).   (3)

12. (a) Simplify the logical expression using K-map in SOP and POS form
$F(A, B, C, D) = \Sigma m(0, 2, 3, 6, 7) + d(8, 10, 11, 15)$. (13)

Or

(b) Design a full subtractor and realise using logic gates. Also, implement the same using half subtractors (13)

13. (a) Design a sequence detector that produces an output '1' whenever the non-overlapping sequence 101101 is detected. (13)

Or

(b) (i) Explain the realization of JK flip flop from T flip flop. (7)

(ii) Write short notes on SIPO and draw the output waveforms. (6)

14. (a) Design an asynchronous circuit that has two inputs $x1$ and $x2$ and one output z. The circuit is required to give an output whenever the input sequence $(0,0)$, $(0,1)$ and $(1, 1)$ received but only in that order (13)

Or

(b) (i) Design a PLA structure using AND and OR logic for the following functions. (10)

$F1 = \Sigma m(0, 1, 2, 3, 4, 7, 8, 11, 12, 15)$

$F2 = \Sigma m(2, 3, 6, 7, 8, 9, 12, 13)$

$F3 = \Sigma m(1, 3, 7, 8, 11, 12, 15)$

$F4 = \Sigma m(0, 1, 4, 8, 11, 12, 15)$

(ii) Compare PLA and PAL circuits. (3)

15. (a) Explain in detail the concept of structural modeling in VHDL with an example of full adder. (13)

Or

(b) (i) Write short notes on built- in operators used in VHDL programming. (6)

(ii) Write VHDL coding for 4×1 Multiplexer. (7)

PART C — $(1 \times 15 = 15$ marks)

16. (a) Assume that there is a parking area in a shop whose capacity is 10. No more than 10 cars are allowed inside the parking area and the gate is closed as soon as the capacity is reached. There is a gate sensor to detect the entry of car which is to be synchronized with the clock pulse. Design and implement a suitable counter using JK flip flops. Also, determine the number of flip flops to be used if the capacity is increased to 50. (15)

Or

(b) Design a 4 bit code converter which converts given binary code into a code in which the adjacent number differs by only 1 by the preceding number. Also, develop VHDL coding for the above mentioned code converter. (15)