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Question Paper Code : 57308

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Third Semester

Electrical and Electronics Engineering

EE 6301 – DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering and Instrumentation and Control Engineering)

(Regulation 2013)

Time : Three Hours

Maximum : 100 Marks

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Convert the following binary code into a Gray Code :

1010111000₂

2. Define fan-in and fan-out.

3. Write the POS representation of the following SOP function :

$$f(x, y, z) = \sum m(0, 1, 3, 5, 7)$$

4. Design a half subtractor.

5. Give the characteristic equation and characteristic table of SR flip-flop.

6. State any two differences between Moore and Mealy state machines.

7. What are the two types of asynchronous sequential circuits ?

8. State the difference between PROM, PLA and PAL.

9. What is data flow modelling in VHDL ? Give its basic mechanism.

10. Write the VHDL code to realize a 2 × 1 multiplexer.

PART – B (5 × 16 = 80 Marks)

11. (a) (i) Convert 1010111011101100_2 into its octal, decimal and hexadecimal equivalent. (6)
(ii) Deduce the odd parity hamming code for the data : 1010. Introduce an error in the LSB of the hamming code and deduce the steps to detect the error. (10)
- OR**
- (b) (i) With circuit schematic explain the operation of a two input TTL NAND gate. (8)
(ii) With circuit schematic and explain the operation and characteristics of a ECL gate. (8)
12. (a) (i) Simplify the following function using Karnaugh Map.
 $f(w, x, y, z) = \sum m(0, 1, 3, 9, 10, 12, 13, 14) + \sum d(2, 5, 6, 11)$ (8)
(ii) Implement the following function using only NAND gates :
 $f(x, y, z) = \sum m(0, 2, 4, 6)$ (8)
- OR**
- (b) (i) Design a BCD to Excess-3 code converter. (8)
(ii) Design a full adder and implement it using suitable multiplexer. (8)
13. (a) (i) Explain the operation of a JK master slave flip flop. (8)
(ii) Design a MOD-5 counter using T Flip Flops. (8)
- OR**
- (b) (i) Design a serial adder using Mealy state model. (8)
(ii) Explain the state minimization using partitioning procedure with a suitable example. (8)
14. (a) (i) What are Static-0 and Static-1 hazards ? Explain the removal of hazards using hazard covers in K-map. (8)
(ii) Explain cycles and races in asynchronous sequential circuits. (8)
- OR**
- (b) (i) What are transition table and flow table ? Give suitable examples. (6)
(ii) Implement the following function using PLA and PAL : (10)
 $f(x, y, z) = \sum m(0, 1, 3, 5, 7)$
15. (a) (i) Explain the various operators supported by VHDL. (8)
(ii) Write the VHDL code to realize a decade counter with behavioural modelling. (8)
- OR**
- (b) (i) Explain functions and subprograms with suitable examples. (6)
(ii) Write the VHDL code to realize a 4-bit parallel binary adder with structural modelling and write the test bench to verify its functionality. (10)