Reg. No. | | | | | | | | | | | | |

Question Paper Code : 51439

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2014..

Fourth Semester

Electrical and Electronics Engineering

EE 2255/EE 46/EC 1261 A/080280029/10133 EE 406 A – DIGITAL LOGIC CIRCUITS

(Regulation 2008/2010)

(Common to PTEE 2255 – Digital Logic Circuits for B.E (Part-Time) Third Semester Electrical and Electronics Engineering – Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. State De Morgan's theorem.

2. Give examples for weighted codes.

3. What is the drawback of SR flipflop?

4. What is a synchronous sequential circuit?

5. What is FPGA?

6. List the factors used for measuring the performance of digital logic families.

7. What is a turing machine?

8. What are the drawbacks in designing asynchronous sequential machines?

9. What are the advantages of hardware languages?

10. Write VHDL code for half adder in data flow model.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Solve using Quine McCluskey method. $\Sigma 1,3,5,7,8,16,20,25,31$. (8)

(ii) Design 3 bit magnitude comparator. (8)

Or

(b) (i) Design 2421 to excess – 3 code converter. (8)

(ii) How can you convert 4 × 16 decoder to 16 × 1 MUX? (8)

12. (a) (i) Construct a JK flipflop using JK flipflop, a 2 × 1 MUX and an inverter. (8)

(ii) A sequential circuit has two JK flipflops A and B, two inputs x and y, and one output z. The equations are

$J_A = Bx + B'y'$; $K_A = B'xy'$

$J_B = A'x$; $K_B = A + xy'$

$z = Ax'y' + Bx'y'$.

Draw the logic diagram and state table. (8)

Or

(b) (i) Design a sequential circuit with two D – flip flops A and B and one input x. When $x = 0$, the state of the circuit remains the same. When $x = 1$, the circuit goes through the state transitions from $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00$ and repeats. (8)

(ii) Design mod 7 counter using D flipflops. (8)

13. (a) (i) Design asynchronous BCD counter using JK flipflops. (8)

(ii) An asynchronous sequential circuit is described by $Y = x_1x_2' + (x_1 + x_2')y$; $z = y$. Draw the logic diagram, transition table and output map. (8)

Or

(b) (i) Find a circuit that has no static harzards and implements boolean function $F(A,B,C,D) = \Sigma(0,2,6,7,8,10,12)$. (8)

(ii) Find a binary state assignment for the reduced flow table below. (8)

	x_1x_2 = 00	01	11	10
a	ⓐ, 0	ⓐ, 1	b, –	d, –
b	a, –	ⓑ, 0	ⓑ, 0	c, –
c	a, –	–, –	d, –	e, –
d	a, –	a, –	d, –	ⓒ, 0
e	a, –	ⓓ, 0	ⓓ, 1	ⓓ, 1

14. (a) (i) Explain the different types of programmable logic devices with neat schematic and compare them. (10)

(ii) Draw an ECL AND gate and explain. (6)

Or

(b) Compare the characteristic features of TTL, ECL, CMOS digital logic families. (16)

15. (a) Write VHDL code for full adder and 8 × 1 multiplexer. (16)

Or

(b) Write VHDL code for JK master slave flipflops and using JK FF as structural element write code for 4 bit Asynchronous counter. (6 + 10)