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Question Paper Code : 71731

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Fourth Semester

Electronics and Communication Engineering

EC 6404 — LINEAR INTEGRATED CIRCUITS

(Common to Medical Electronics Engineering, Robotics and Automation Engineering)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the ideal characteristics of OpAmp.

2. Why is the current mirror circuit used in differential amplifier stages?

3. What is the need for converting a First order Filter into a Second order filter?

4. How is the current characteristic of a PN junction employed in a Log amplifier?

5. How are square root and square of a signal obtained with multiplier circuit?

6. How is frequency stability obtained in a PLL by use of a VCO?

7. An 8 bit A/D converter accepts an input voltage signal of range 0 to 12V. What is the digital output for an input voltage of 6V?

8. Why are Scottky diodes used in sample- and- hold circuits?

9. What is the need for voltage regulator ICs?

10. Distinguish the principle of linear regulator and a switched mode power supply.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Derive the functional parameters for an Inverting mode negative feedback gain circuit with a 741 OpAmp in IC Inverting mode, with R1= 1 Kohm, Rf = 40 Kohm and Compute Af; Rif; Rof; BW; offset voltage.

(ii) Discuss briefly on the differential mode Instrumentation amplifier. (7+6)

Or

(b) (i) What is input and output voltage and current offsets? How are they compensated?

(ii) With neat diagram derive the AC performance close loop characteristics of OpAmp to discuss on the circuit Bandwidth, Frequency response and slewrate. (7+6)

12. (a) With neat figures describe the circuit using OpAmps on the functioning of

(i) Integrator and double integrator circuit

(ii) First order High pass filter. (7+6)

Or

(b) With neat figures describe the circuit using OpAmps on the operation of

(i) Zerocross Detecter, Clipper and clamper circuits

(ii) Scmitt Trigger. (7+6)

13. (a) With neat diagram explain the design of (i) Frequency Synthesizer (ii) Frequency Division circuit using PLL IC 565. (7+6)

Or

(b) With neat figures explain the emitter couple circuit based design of (i) Gilbert multiplier cell for four quadrant multiplication (ii) the operation of VCO. (7+6)

14. (a) (i) How are A/D converters categorized?

(ii) Discuss on the successive approximation type ADC. (6+7)

Or

(b) (i) What is meant by resolution, offset error in ADC.

(ii) Discuss on the dual slope type ADC. (6+7)

15. (a) Describe the 555 Timer IC. Design a Astable Multivibrater Circuit to generate output Pulses of 25%, 50% duty cycle using a 555 Timer IC, with choice of $C = 0.01\,\mu F$, Frequency as 4.0 KHz. (13)

Or

(b) Answer any two of the following:

(i) Switched capacitor filters.

(ii) Audio power amplifier.

(iii) Opto coupler. (7+6)

PART C — ($1 \times 15 = 15$ marks)

16. (a) With a neat block diagram explain the stages for developing the signal analysis circuits required for an instrumentation module of say a vibration sensor data using instrumentation amplifier, wave shaper, comparator and ADC using OPAMP and required components.

Or

(b) With a neat figures design a PLL with free running frequency of 500 kHz and the bandwidth of low pass filter is 50 kHz. Will the loop acquire lock for an input signal of 600 kHz. Justify your answer. Assume that phase detector needs to produce sum and difference frequency components.
