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## Question Paper Code : 97066

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Third Semester

## Electrical and Electronics Engineering EE 6303 - LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

(Common to Electronics and Instrumentation Engineering and Instrumentation and Control Engineering)
(Regulation 2013)
Time : Three hours
Maximum : 100 marks
Answer ALL questions.
PART A - $(10 \times 2=20 \mathrm{marks})$

1. What are the major categories of Integrated Circuits?
2. Mention the advantages of Integrated circuits over discrete circuits.
3. Draw an adder circuit using an op-amp to get the output expression as $V_{0}=-\left(0.1 V_{1}+V_{2}+10 V_{3}\right)$ where $V_{1}, V_{2}$ and $V_{3}$ are the inputs.
4. A 100 pF capacitor has a maximum charging current of 150 microamps. What is the slew rate?
5. Draw the fundamental sample and hold circuit. What is the purpose of $\mathrm{S} / \mathrm{H}$ in data converters?
6. How many comparators are required to design a 10 bit flash ADC ?
7. A PLL frequency multiplier has an input frequency of. " $f$ " and a decade counter is included in the loop. What will be the frequency of the PLL output?
8. What are the advantages of variable transconductance technique?
9. What is meant by thermal shutdown applied to voltage regulators?
10. Draw the internal block diagram of a function generator IC.
11. (a) (i) Explain the fabrication process involved in the following circuit diagram (Figure 1).


Figure 1
(ii) Explain the process of masking and photo etching in IC fabrication. Or
(b) (i) Discuss the different ways to fabricate diodes.
(ii) Explain how a monolithic capacitor can be fabricated.
12. (a) (i) Consider the lossy integrator as shown in figure 2. For the component values $\mathrm{R}_{1}=10 \mathrm{k} \Omega, \mathrm{R}_{\mathrm{f}}=100 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{f}}=1 \mathrm{nF}$, Determine the lower frequency limit of integration and study the response for the inputs
(1) step input
(2) square input
(3) sine input.


Figure 2
(ii) Design an adder-subtrator circuit for $\mathrm{V}_{0}=2 \mathrm{~V}_{1}+5 \mathrm{~V}_{2}-10 \mathrm{~V}_{3}$.

Or
(b) (i) For a V-I convertor shown in figure $3, \mathrm{~V}_{\mathrm{in}}=5 \mathrm{~V}, \mathrm{R}=10 \mathrm{~K} \Omega$, $\mathrm{V}_{1}=1 \mathrm{~V}$, find the load current and output voltage $\mathrm{V}_{0}$. Assume the op-amp is initially mulled.

*Figure 3
(ii) For a max frequency of 100 Hz , design a differentiator circuit and draw the frequency response for the same.
13. (a) (i) A dual slope ADC uses 16 -bit counter and 4 MHz clock rate. The maximum input voltage is +10 V . The maximum integrator output voltage should be -8 V when the counter has cycled through $2^{n}$ counts. The capacitor used in the integrator is $0.1 \mu \mathrm{~F}$. Find the value of resistor $R$ of the integrator.
(ii) Derive the expression for the $\log$ and antilog amplifiers with necessary diagrams.

Or
(b) (i) In a triangular wave generator given $R_{2}=1.2 \mathrm{k} \Omega$, $R_{3}=6.8 k \Omega, R_{1}=120 \mathrm{k} \Omega, C_{1}=0.01 \mu F$. Determine the peak to peak op amplitude of triangular wave and frequency of the triangular wave.
(ii) Design a RC phase shift oscillator for a frequency of 1 KHz .
14. (a) (i) For the VCO circuit, assume $R_{2}=2.2 \mathrm{~K} \Omega, \mathrm{R}_{1}=\mathrm{R}_{3}=15 \mathrm{~K} \Omega$ and $\mathrm{C}_{1}=0.001 \mathrm{uF}$. Assume $\mathrm{V}_{c c}=12 \mathrm{~V}$. Determine the output frequency, the change in output frequency if modulating input $\mathrm{V}_{\mathrm{c}}$. is varied from 7 V to 8 V .
(ii) For a 555 astable circuit, determine the high state time interval, low state time interval, period, frequency and duty cycle.

Or
(b) With neat diagram, explain the operation of four quadrant variable transconductance multiplier circuit.
15. (a) (i) State the advantages of IC voltage. Explain the features and internal structure of general purpose Linear IC 723 regulator. Design a regulator using IC 723 to meet the following specifications: $\mathrm{V}_{0}=5 \mathrm{~V} ; \mathrm{I}_{0}=100 \mathrm{~mA} ; \mathrm{V}_{\mathrm{in}}=15 \pm 20 \% ; \mathrm{I}_{\mathrm{sc}}=150 \mathrm{~mA}$; $\mathrm{V}_{\text {sense }}=0.7 \mathrm{~V}$
(ii) With a neat diagram, explain the working of step down switching regulator.

## Or

(b) (i) With a neat functional diagram, explain the operation of LM 380 power amplifier.
(ii) Explain the operation of SMPS with neat diagrams.

