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## Question Paper Code : 41235

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Sixth Semester<br>Electrical and Electronics Engineering<br>080280051 - DIGITAL SIGNAL PROCESSING

(Common to B.E.(Part-Time) Fifth Semester Electrical and Electronics Engineering)
(Regulation 2008)

Time : Three hours
Maximum : 100 marks

> Answer ALL questions.
> PART A $-(10 \times 2=20$ marks $)$

1. Give the functional and wave form representation of unit impulse, unit step, and unit ramp.
2. State the sampling theorem.
3. Write the condition for stability in terms of impulse response of a system.
4. Brief up the properties of region of convergence in Z transform.
5. Write the relationship between Z transform and DFT with expressions.
6. State and prove shifting property of DFT.
7. How many multiplications and additions are involved in radix-2 FFT algorithm?
8. What is 'Gibbs' phenomenon?
9. Compare and contrast impulse invariant and bilinear transformation techniques.
10. Distinguish between Van Neumann and Harvard architectures.

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\text { PART B }-(5 \times 16=80 \text { marks })
$$

11. (a) (i) Determine whether the system having input $x(n)$ and output $y(n)$ and described by relationship : $y(n)=\sum_{K=-\infty}^{n} x(k+2)$ is (1) memoryless, (2) stable, (3) causal (4) linear and (5) time invariant.
(ii) Explain the successive approximation type analog to digital converter with diagrams.

Or
(b) (i) Discuss about the various types of digital signal processing operations with examples.
(ii) What is the input signal $x(n)$ that will generate the output sequence $y(n)=\{1,-1,0,2,-2,1\}$ for a Linear Time Invariant system with impulse response of $\dot{h}(n)=\{1,1,1\}$.
12. (a) (i) Obtain the $z$ transforms and hence the regions of convergence of the following sequences.

$$
\begin{equation*}
x(n)=[u(n)-u(n-10)] 2^{-n} \tag{1}
\end{equation*}
$$

(2) $\quad x(n)=\cos (\pi n) \cdot u(n)$.
(ii) Consider a stable causal. LTI system whose input $x(n)$ and output $y(n)$ are related through second order difference equation, $y(n)-\left(\frac{3}{4}\right) y(n-1)+\frac{1}{8} y(n-2)=2 x(n)$. Determine the response for the given input $x(n)=(1 / 4)^{n} u(n)$ using DTFT.

## Or

(b) (i) A second order discrete time system is characterized by the difference equation.
$y(n)-0.1 y(n-1)-0.02 y(n-2)=2 x(n)-x(n-1)$.
Find $y(n)$ for $0 \geq n$ when $x(n)=u(n)$ and the initial conditions are given as $y(-1)=-10, y(-2)=20$.
(ii) Find the Z-Transform $\mathrm{X}(\mathrm{z})$ " and sketch the pole-zero plot with the ROC for each of the following sequences.

$$
\begin{align*}
& x(n)=\left(\frac{1}{2}\right)^{n} u(n)+\left(\frac{1}{3}\right)^{n} u(n)  \tag{1}\\
& x(n)=\left(\frac{1}{3}\right)^{n} u(n)-\left(\frac{1}{2}\right)^{n} u(-n-1) \tag{2}
\end{align*}
$$

13. (a) (i) Find the IDFT of the sequence

$$
\begin{equation*}
X(k)=\{2,0.5-j 1.207,0,0.5-j 0.207,0,0.5+j 0.207,0,0.5+j 1.207\} \tag{10}
\end{equation*}
$$ using Radix-2 DIF -FFT algorithm.

(ii) Write a detailed technical note on the wavelet transform and its applications.

Or
(b) (i) Let $\mathrm{X}(\mathrm{k})$ is the N -point DFT of a sequence $\mathrm{x}(\mathrm{n})$ with N even. Define two sequences of length $N / 2$ given by,

$$
\begin{align*}
& f(n)=(1 / 2)[x(2 n)+x(2 n+1)] \\
& g(n)=(1 / 2)[x(2 n)-x(2 n+1)] \tag{6}
\end{align*}
$$

(ii) Derive the computational steps of 8-point radix-2 DIT-FFT algorithm and draw the signal flow diagram.
14. (a) Design an IIR Butterworth digital low pass filter satisfying the following specification.

Sampling time $=1 \mathrm{sec}$
PB frequency $=.0 .055 \pi \mathrm{rad} / \mathrm{sec}$
SB frequency $=0.65 \mathrm{rad} / \mathrm{sec}$
PB Attenuation $=7 \mathrm{~dB}$
SB Attenuation $=25 \mathrm{~dB}$.
Or
(b) Design an FIR digital filter with

$$
\begin{align*}
H_{d}\left(e^{j \omega}\right) & =e^{-j 5 \omega} ;-\pi / 2 \leq \omega \leq \pi / 2 \\
& =0 ; \quad \pi / 2<\omega \leq \pi \tag{16}
\end{align*}
$$

Using Blackman window with $\mathrm{N}=11$.
15. (a) Discuss in detail about the various addressing modes of TMS320C54X processor.

Or
(b) Explain the architecture of TMS320C54X processor with appropriate diagram.

