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Question Paper Code : 52919

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Fourth/Fifth Semester

Electronics and Communication Engineering

EC 6504 — Microprocessor and Microcontroller

(Common to Biomedical Engineering/Computer Science and Engineering/Medical Electronics/Information Technology)

(Regulation 2013)

(Also common to : PTEC 6504 – Microprocessor and Microcontroller for B.E. (Part-Time) – Third Semester – Computer Science and Engineering – Fourth Semester – Electronics and Communication Engineering – Regulation 2014)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Given that (BX) = 0158 (DI) = 10A5 Displacement = 1B57 (DS) = 2100. Determine the effective address and physical address for the following addressing modes.
   (a) Register Indirect
   (b) Relative based indexed.
2. What are macros?
3. Draw the format of the Flag register.
4. Write the advantages of loosely coupled system over tightly coupled systems.
5. What is mode 0 operation of 8255?
6. What are the operating modes in 8279?
7. Which bits of the PSW are responsible for selection of the register banks?

8. For an 8051 system of 11 .0592 MHz, find the time delay for the following subroutine:

		Machine Cycle
DELAY:	MOV R3, #250	1
HERE:	NOP	1
	NOP	1
	NOP	1
	NOP	1
	DJNZ, R3, HERE	2
	RET	2

9. What are the different modes in which timer 2 can operate?

10. When is an external memory access generated in 8051?

PART B — (5 × 13 = 65 marks)

11. (a) With neat block diagram, explain the architecture of 8086 Microprocessor.

Or

(b) What is Interrupt and interrupt routine. Explain interrupt sequence for 8086 Microprocessor and interrupt pointers.

12. (a) With neat block diagram, explain the architecture of 8086 in maximum mode configuration. Also explain the Bus timing diagram for input and output transfer on a maximum mode.

Or

(b) Explain the interrupt system based on multiple 8259 with necessary block diagram.

13. (a) Draw the Block diagram and explain the operations of 8251 serial communication interface.

Or

(b) Explain in detail about interfacing of four LCD digits to 8086.

14. (a) (i) Explain in detail about the 8051 register banks and stack. (8)

(ii) Show the code to push R5, R6 and A onto the stack and then pop them back into R2, R3, and B, where register B = register A, R2 = R6, and R3 = R5. (5)

Or

(b) Briefly explain about the various addressing modes of 8051 with one example.

15. (a) Describe how to program and interface an LCD to an 8051 using Assembly language programming.

Or

(b) Draw and explain the DAC interfacing using 8051.

PART C — (1 × 15 = 15 marks)

16. (a) (i) Discuss what happens if interrupts INTO, TFO, and INT1 are activated at the same time. Assume priority levels were set by the power-up reset and that the external hardware interrupts are edge-triggered. (7)

(ii) With necessary diagrams explain how to interface LM35 temperature sensor and then discuss the issues of signal conditioning. (8)

Or

(b) (i) Discuss the number of pin sets aside for addresses in each of the following memory chips. (1) 16K × 4 DRAM and (2) 16 K × 4 SRAM. (4)

(ii) Briefly explain about the interfacing of 8051 with external data ROM. (11)