Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 41263

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Fifth Semester

Electronics and Communication Engineering

080290030 – MICROPROCESSORS AND APPLICATIONS

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Give the priority order of 8085 interrupts.
2. What is the difference between SUB and CMP instruction of 8085?
3. List the segment registers of 8086.
4. How queue is implemented in 8086?
5. How do you evaluate the 20 bit address if the registers are 16 bit wide?
6. What is the difference between arithmetic shift and logical shift?
7. Distinguish decoded and encoded scan modes of 8279.
8. What is the need for GATE signal in 8254?
9. What are the advantages of programmed I/O?
10. What is the need for DMA?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Draw the timing diagram of 8085 instruction "STA addr 16" and explain. (12)

(ii) What are differences between CMP and Sub and JUMP and CALL. (4)

Or

(b) Write an 8085 assembly language program to find the 7 – segment LED code for a 2 – digit BCD data, by using look up table. The BCD data is stored in 4200 H. Store the 7 – segment code in 4201 H and 4202 H.

12. (a) Explain the organization of interrupt vector table in 8086 and servicing an interrupt by 8086.

Or

(b) Distinguish Maximum and Minimum mode 8086 CPU module.

13. (a) Write an 8086 assembly language program to determine the GCD of two 16 – bit data.

Or

(b) Explain XLAT, CBW, STOS and LOCK instructions of 8086 with example.

14. (a) (i) Explain the Internal block diagram of 8255. (8)

(ii) Discuss the I/O modes of 8255. (8)

Or

(b) With schematic diagram explain Interfacting DAC 0800 with 8086 microprocessor.

15. (a) Explain in detail how SRAM and DRAM are interfaced?

Or

(b) Write notes on :

(i) Memory mapped I/O and I/O mapped I/O

(ii) Optical motor shaft encoders.

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