Reg. No. :

Question Paper Code : X65650

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Sixth Semester
Electronics and Communication Engineering
080290038 – VLSI DESIGN
(Regulations 2008)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. What is latch up ? How is it prevented ?
2. What are the four types of design rules ?
3. What is the impact of body effect in CMOS inverter ?
4. Write the standard SPICE syntax for MOSFET (level 1).
5. Draw the layout of tristate inverter and give its significance.
6. How does transmission gates act as switch ?
7. Sketch a basic SRAM cell.
8. Define self-resetting logic.
9. Write a VHDL code for a positive edge triggered D Flip Flop.
10. What is a package in VHDL ? State its significances.

PART – B **(5×16=80 Marks)**

11. a) i) Explain with a neat diagram the n-well CMOS process of fabrication highlighting the steps involved. **(8)**

ii) Explain the different types of Contact Cuts between polysilicon and diffusion layer in nMOS circuits along with their dimensional details. **(8)**

(OR)

b) i) Describe the steps involved in nMOS transistor fabrication process. Illustrate with neat diagrams the steps involved. **(8)**

ii) Explain the λ based transistor design rules for nMOS and CMOS transistors. **(8)**

12. a) i) Derive the relationship between drain to source current Ids and drain to source voltage Vds in non saturation and saturation region. **(8)**

ii) A CMOS inverter is built in a process where k′n = 100 μA/V^2, V_{tn} = +0.7V, k′p = 42 μ A/V^2, V_{tp} = –0.8V, and a power supply of V_{DD} = 3.33V is used. Find mid point voltage VM if $(W/L)_n$=10 and$(W/L)_p$ = 14. **(8)**

(OR)

b) i) Derive an equation for transconductance of an n-channel enhancement MOSFET operating in active region. **(8)**

ii) Discuss the Switch model and Square law model of MOSFET. **(8)**

13. a) i) Synthesis the complex function $g = \overline{a.b + c.d}$ Using CMOS gates. **(10)**

ii) Write short notes on large FETS. **(6)**

(OR)

b) i) Synthesis 2 input XOR gate using transmission gates. **(6)**

ii) Design half adder and full adder cell and create a CMOS cell for the logic function $F = \overline{a + (b + c) + (d + e)}$. **(10)**

14. a) i) With a neat layout diagram explain the static RAM 6T cell and its writing and reading operations. **(8)**

ii) Describe the central SRAM block architecture along with the operation of the row driver circuit. **(8)**

(OR)

b) i) With the diagram explain the write and hold operations of a 1T DRAM cell. How is refresh operation carried out in a DRAM cell ? **(8)**

ii) Explain the operation of a non-inverting domino logic gate long with its layout **(8)**

15. a) Write a behavioural VHDL program for realizing an 8 bit shift register that could be configured to perform serial to parallel and parallel to serial shift logics.

(OR)

b) i) Draw the VHDL design flow model and explain the significance of each steps. **(8)**

ii) Write a structural VHDL program for a 4 to 16 decoder circuit. **(8)**