Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 80459

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Sixth/Eight Semester

Electronics and Communication Engineering

EC 2354/EC 64/10144 EC 704 – VLSI DESIGN

(Common to Biomedical Engineering)

(Regulations 2008/2010)

(Also Common to PTEC 2354 – VLSI Design for B.E. (Part-Time) Fifth Semester – Electronics and Communication Engineering – Regulations 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the various issues in Technology-CAD.

2. Define the lambda layout rules.

3. State the types of power dissipation.

4. Define Scaling. What are the advantages of scaling?

5. Differentiate between latch and flipflop.

6. List out the techniques used for low power logic design.

7. Distinguish testers and test fixtures.

8. What are the stages at which a chip can be tested?

9. Differentiate blocking and non-blocking assignments.

10. Mention the possible values which are allowed in Verilog HDL.

PART B — (5 × 16 = 80 marks)

11. (a) Explain in detail about the ideal I-V characteristics and non ideal I-V characteristics of a NMOS and PMOS devices. (16)

Or

(b) (i) Explain in detail about the body effect and its effect in NMOS and PMOS devices. (8)

(ii) Derive the expression for DC transfer characteristics of CMOS inverter (8)

12. (a) (i) Explain the different factors that affects the reliability of CMOS chips. (10)

(ii) Discuss the principle of constant field and lateral scaling. Write the effects of the above scaling methods on the device characteristics. (6)

Or

(b) (i) Discuss the mathematical equations that can be used to model the drain current and diffusion capacitance of MOS transistors. (8)

(ii) Give a brief note an logical effort and transistors sizing. (8)

13. (a) (i) Implement $Y = (A + B)(C + D)$ using the standard CMOS logic. (8)

(ii) Implement NAND gate using pseudo-nMOS logic. (8)

Or

(b) (i) Implement D-fIip-flop using transmission gate. (8)

(ii) Implement a 2-bit non-inverting dynamic shift register using pass transistor logic. (8)

14. (a) Briefly discuss the following terms: (16)

(i) Testers

(ii) Test fixtures

(iii) Test programs

Or

(b) (i) Explain the Silicon debug principles in detail (8)

(ii) Explain the manufacturing test principles in detail (8)

15. (a) Explain how to represent the gate delays in Verilog HDL with an example.

Or

(b) (i) Write a Verilog code for D-flip-flop. (8)

(ii) Explain blocking and non-blocking assignments (8)

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