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Question Paper Code : 20421

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Sixth/Seventh/Eighth Semester

Electronics and Communication Engineering

EC 6601 — VLSI DESIGN

(Common to Electrical and Electronics Engineering, Biomedical Engineering, Electronics and Instrumentation Engineering, Medical Electronics, Robotics and Automation engineering)

(Regulations 2013)

(Also Common to PTEC 6601 — VLSI Design for B.E. (Part-Time) Fifth Semester – Electronics and Communication Engineering and Third Semester – Electrical and Electronics Engineering – Regulation 2014)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Why NMOS device conducts strong zero and weak one?

2. Draw the stick diagram of static CMOS 2-input NAND gate.

3. Determine the discharging time of the circuit shown in Figure-1. when switch 'A' is closed.

   Assume C_L and internal capacitances C_1 and C_2 are charged initially. Let

   $C_L = C_1 = C_2 = C$.

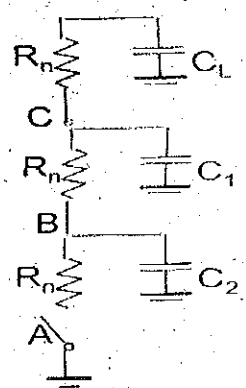

Fig 1

4. Realize X = B+ C and $Y = (A.(B + C))$ using multiple output domino stages.

5. List out the advantages and limitations of 3 T DRAM over 1 T DRAM.

6. List out the advantage of C²MOS logic based register over pass-transistor logic based master-slave register.

7. The circuit in Fig.2 shows a carry propagation path in an adder circuit. Let A,B.C_i are the inputs to adder circuit and φ is the clock signal. Write the logic expressions for the signal X, Y to generate output carry.

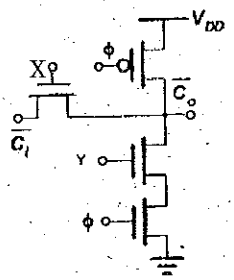

Fig. 2

8. Draw a 4-bit ripple carry adder and find its critical path delay.

9. Compare between Xilinx CLB interconnect and Alter a LAB interconnect.

10. Differentiate between full custom design and semi custom design.

PART B — (5 × 13 = 65 marks)

11. (a) (i) List out the goals of CMOS technology scaling. Explain How common electric field scaling is superior than constant voltage scaling. (7)

(ii) Derive the expression to obtain the minimum delay through the chain of CMOS inverter. (6)

Or

(b) (i) Explain the design techniques that are used for larger fan-in devices to reduce delay. (8)

(ii) Draw the small signal model of device during cut-off, linear and saturation region. (5)

12. (a) (i) Implement the equation $X = \overline{(A + B)CD}$ using complementary CMOS logic.

(1) Size the devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 4 and PMOS W/L = 8.

(2) What are the input patterns that give the worst case t_{PHL} and t_{PLH}. Consider the effect of the capacitances at the internal nodes.

(3) If $P(A=1)=0.5$, $P(B=1)=0.2$, $P(C=1)=0.3$, $P(D=1)=1$, determine the power dissipation in the logic gate. Assume $V_{DD}=2.5V$, $C_{out}=30\,fF$ and $F_{clk}=250$ MHz. (7)

(ii) List out the limitations of pass transistor logic. Explain any two techniques used to overcome the drawback of pass transistor logic design. (6)

Or

(b) (i) Explain in detail the signal integrity issues in dynamic logic design. propose any two solutions to overcome it. (7)

(ii) (1) Determine the truth table for the circuit shown Figure-3. What logic function does it implement? (4)

(2) If the PMOS were removed, would the circuit still function correctly? Does the PMOS transistor serve any useful purpose? (2)

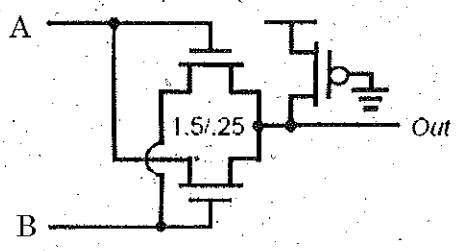

Fig 3

13. (a) (i) Identify the type of register for the circuit shown in figure 4 and express set up time, hold time and propagation delay of register in terms of the propagation delay of inverters and transmission gates. (5)

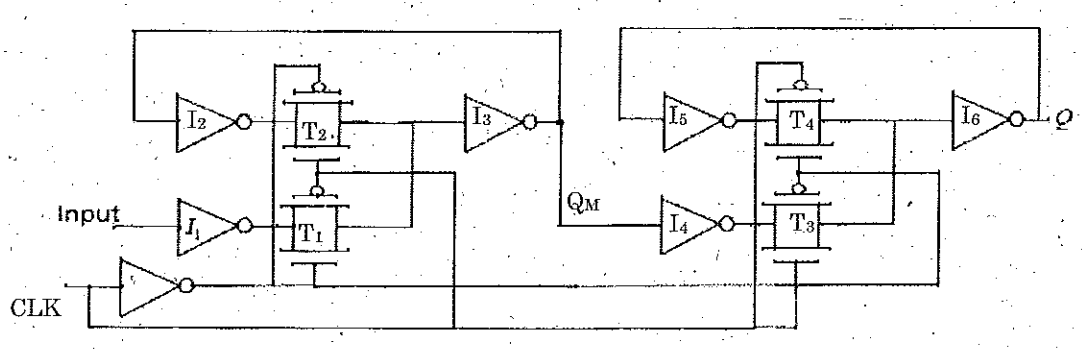

Fig. 4

(ii) Implement the register of question 13(i) using C²MOS logic and explain how 0-0 and 1-1 overlap of clock signals are eliminated. (8)

Or

(b) (i) Construct 6T based SRAM cell. Explain its read and write operations. What is the importance of Cell ratio and Pull up ratio in 6T SRAM cell? (8)

(ii) Analyze the impact of spatial variations of clock signal on edge-triggered sequential logic circuits. (5)

14. (a) Design an 8-bit Brent-Kung Adder. (13)

Or

(b) (i) Construct 4 × 4 Array type multiplier and find its critical path delay. (8)

(ii) Design 4-input and 4-output barrel shift adder using NMOS logic. (5)

15. (a) Explain CLB of Xilinx 4000 architecture. (13)

Or

(b) (i) Realize the function, $F = A.B + (B'C) + D$ using ACTEL (ACT-1) FPGA. (5)

(ii) Draw the flow chart of digital circuit design techniques. (4)

(iii) Differentiate between Hard Macro and Soft Macro. (4)

PART C — (1 × 15 = 15 marks)

16. (a) Derive an expression to show the drain current of MOS for various operating region. Explain one non-ideality for each operating region that changes the drain current. (15)

Or

(b) Explain in detail the CMOS manufacturing process. (15)

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