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# Question Paper Code : X 20453

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Sixth/Seventh/Eighth Semester
Electronics and Communication Engineering
EC 6601 – VLSI DESIGN
(Common to Biomedical Engineering/Electrical and Electronics Engineering/
Electronics and Instrumentation Engineering/Medical Electronics Engineering/
Robotics and Automation Engineering – Regulations 2013)
(Common to PTEC 6601 – VLSI Design – for B.E. (Part-Time) Sixth Semester
For Electronics and Communication Engineering and Seventh Semester for
Electrical and Electronics Engineering – Regulations 2014)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Compare PMOS and NMOS.
2. State the need for scaling.
3. Draw the circuit of XOR using transmission gate.
4. Mention some of the techniques to minimize power dissipation.
5. Draw the circuit of 1-bit inverting register using NMOS pass transistor logic.
6. Compare DRAM and SRAM.
7. Define propagate, generate and kill terms in an adder.
8. State the merits of barrel shifter.
9. Mention the important functional blocks in an FPGA.
10. Compare full-custom and semi-custom design.

PART – B **(5×13=65 Marks)**

11. a) Derive an expression for $I_{ds}$ and $g_m$ in the linear and in the saturated region. **(13)**

(OR)

b) Draw the circuit of NOR gate using NMOS and using static CMOS logic. Also draw the corresponding stick diagram. **(13)**

12. a) i) Realize the following Boolean function Z = (A + BC)D + E using static CMOS logic. **(6)**

ii) Realize the 8 : l multiplexer using 4 : l and 2 : l multiplexer. Draw the realization using transmission gate. **(7)**

(OR)

b) Define power dissipation. State the different types of power dissipation. Derive an expression for dynamic power dissipation. **(13)**

13. a) Draw the circuit of D-latch using transmission gate. Using D-latch realize the master-slave D-flip-flop using transmission gate and explain its working. **(13)**

(OR)

b) Draw the circuit of 6-transistor SRAM cell using NMOS. Explain the read and write operation. **(13)**

14. a) Derive the Boolean expression for sum and cout of a 4-bit carry look ahead adder. Draw the realization of cout using Dynamic CMOS logic. **(13)**

(OR)

b) State radix-2 booth encoding. Apply radix-2 booth encoding to perform the multiplication operation between (–4) and (3). Assume it is a 4-bit multiplier. **(13)**

15. a) With neat diagram, elucidate the architecture of FPGA. **(13)**

OR

b) Explain the interconnecting resources of FPGA in detail. **(13)**

PART – C **(1×15=15 Marks)**

16. a) With neat diagram, describe the architecture of 4 × 4 unsigned array multiplier. **(15)**

(OR)

b) Derive an expression for the rise time, fall time and the propagation delay of a CMOS inverter. **(15)**

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