Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 70440

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Sixth/Seventh/Eighth Semester

Electronics and Communication Engineering

EC 6601 – VLSI DESIGN

(Common to Biomedical Engineering/Electrical and Electronics Engineering/ Electronics and Communication Engineering/Electronics and Instrumentation Engineering/Medical Electronics Engineering/Robotics and Automation Engineering)

(Regulations 2013)

(Also Common to : PTEC 6601 – VLSI DESIGN for B.E. (Part-Time) – Electronics and Communication Engineering/Electronical and Electronics Engineering/Fifth, Seventh Semester (Regulations – 2014)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. What is meant Channel length modulation in NMOS transistors?

2. Define propagation delay of a CMOS inverter.

3. Give Elmore delay expression for propagation delay of an inverter.

4. Why single phase dynamic logic structure cannot be cascaded? Justify.

5. What is meant by pipelining?

6. Draw the schematic of dynamic edge-triggered register.

7. The circuit in Fig.Q.7 shows a carry propagation path in an adder circuit. Let $A,B.C_i$ are the inputs to adder circuit and φ is the clock signal. Write the logic expressions for the signal X, Y to generate output carry.

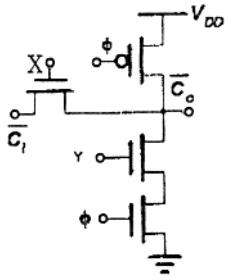


Fig.Q.7

8. Draw a 4-bit ripple carry adder and find its critical path delay.

9. What is the role of cell libraries in ASIC design?

10. What are the two different types of routing?

PART B — ($5 \times 13 = 65$ marks)

11. (a) (i) Explain the different steps involved in n-well CMOS fabrication process with neat diagrams. (9)

(ii) Derive the noise margins for a CMOS inverter (4)

Or

(b) (i) Discuss in detail with a neat layout, the design rules for a CMOS inverter. (6)

(ii) Discuss the mathematical equations that can be used to model the drain current and diffusion capacitance of MOS transistors. (7)

12. (a) (i) Draw the static CMOS logic circuit for the following expression (6)

(1) $Y = \left(\overline{A \cdot B \cdot C \cdot D}\right)$

(2) $Y = \overline{D(A + BC)}$

(ii) Discuss in detail the characteristics of CMOS transmission gate? (7)

Or

(b) What are the sources of power dissipation in CMOS and discuss various design techniques to reduce power dissipation in CMOS? (13)

13. (a) Explain the operation of master-slave based edge triggered register. (13)

Or

(b) Discuss in detail various pipelining approaches to optimize sequential circuits. (13)

14. (a) (i) Explain the concept of carry look ahead adder with neat diagram. (7)

(ii) Discuss the details about speed and area trade off. (6)

Or

(b) Explain the concept of modified Booth multiplier with a suitable example. (13)

15. (a) Explain CLB of Xilinx 4000 architecture (13)

Or

(b) (i) Realize the function. $F = A.B + (B'C) + D$ using ACTEL (ACT-1) FPGA. (5)

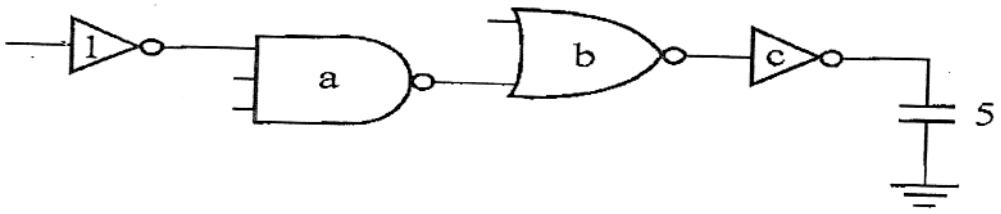
(ii) Draw the flow chart of digital circuit design techniques. (4)

(iii) Differentiate between Hard Macro and Soft Macro (4)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Design a CMOS logic circuit for the given expression $X = [(A + B) \cdot (C + D)]'$ and draw its stick diagram. (7)

(ii) Obtain the logical effort and path efforts of the given circuit. (8)



Or

(b) (i) Design a clock distribution network based on H tree model for 16 nodes. (7)

(ii) Design a four input NAND gate and obtain its delay during the transition from high to low. (8)

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