Reg. No. : | | | | | | | | | | | | |

Question Paper Code : X65631

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Seventh Semester
Electrical and Electronics Engineering
080280062 – VLSI DESIGN
(Regulations 2008)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. State the difference between enhancement and depletion mode MOS transistors.
2. List the major advantages of submicron technology.
3. What is the need for design rules ?
4. Define sheet resistance.
5. List the advantage of transmission gates over pass transistor.
6. What is dynamic CMOS logic ?
7. What are the primary factors involved in the choice of a PAL device for designing digital circuits ?
8. What is the need for slew rate control for the output signals of CPLD's and FPGAs ?
9. Write down the statement for signal assignment using VHDL.
10. What is the purpose of test bench in a VHDL design environment ?

PART – B **(5×16=80 Marks)**

11. a) i) Explain the operation and characteristics of NMOS transistors with neat diagrams and necessary equations for the drain current in the different regions of operation. **(10)**

ii) An NMOS transistor has the following parameters : gate oxide thickness = 12nm, relative permittivity of gate oxide = 3.9, electron mobility = 540 cm^2/V-sec, threshold voltage 0.7 V, permittivity of free space = 8.85×10^{-14} F/cm and (W/L) = 8. Calculate the drain current when (V_{GS} = 2V and V_{DS} = 1.2V) and (V_{GS} = 2V and V_{DS} = 2.2V). Note that W and L refer to the width and length of the channel respectively. **(6)**

(OR)

b) i) Explain the major steps in twin tub CMOS fabrication process with neat diagrams and write the advantages of this process over p-well and n-well processes. **(12)**

ii) Write the equation for threshold voltage of NMOS transistor and discuss the different factors affecting it. **(4)**

12. a) i) Explain the CMOS layout design rules considering two input NAND gate as an example. **(10)**

ii) Illustrate the computation of sheet resistance and area capacitance using suitable examples. **(6)**

(OR)

b) i) Explain the switching characteristics of CMOS inverter with suitable diagrams and expressions for the rise and fall times. **(12)**

ii) Define latchup and suggest some remedies for this problem. **(4)**

13. a) i) Design a clocked CMOS circuit for the logic expression $Y = \left(\overline{AB + CE}\right)D'$. **(8)**

ii) Design a Half adder circuit using nMOS transistor. **(8)**

(OR)

b) i) Design a CMOS shift register using single phase clock. Also describe the problems associated with single phase clocking scheme. **(10)**

ii) Discuss the advantages of two phase clocking scheme as compared to single phase clocking scheme. **(6)**

14. a) i) Implement a 4 bit barrel shifter using suitable PAL. **(8)**

ii) Explain the architecture of a CPLD. **(8)**

(OR)

b) Discuss with neat sketch, the CLB and I/O block of a Xilinx 4000 series FPGA. **(16)**

15. a) i) What is meant by component instantiation ? What are the methods used for component instantiations ? Give example. **(8)**

ii) Write a VHDL code for a 4 bit up down counter. **(8)**

(OR)

b) i) Explain the operating principle of a 7 segment Decoder and write a VHDL code for the same. **(8)**

ii) Write a VHDL code for an 8 bit shift register. **(8)**

———————