Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 41268

B.E./B.Tech DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Sixth Semester

Electronics and Communication Engineering

080290038 — VLSI DESIGN

(Common to Medical Electronics Engineering)

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is Channel-length modulation?

2. What is the need of photo resist in photolithography?

3. Why is resistor pull up not used in MOS circuits?

4. What is Latch-up? How latch-up problem can be avoided in MOSFET devices.

5. Draw a CMOS circuit for a NAND2 gate.

6. Compare between CMOS and transmission gates.

7. Draw the 6-T SRAM cell.

8. What is dynamic memory?

9. Write a VHDL code for a positive edge triggered D Flip Flop.

10. What is a package in VHDL? State its significances.

PART B — (5 × 16 = 80 marks)

11. (a) With neat sketches, explain in detail, all the steps involved in fabrication of an inverter using Silicon On Insulator Process.

Or

(b) (i) Write a technical note on Lambda based rules for CMOS design. (8)

(ii) Draw the layout diagram for a NAND3 Gate. (8)

12. (a) (i) Derive the relationship between drain to source current Ids and drain to source voltage Vds in non saturation and saturation region. (8)

(ii) A CMOS inverter is built in a process where $k'n = 100\ \mu A/V^2$, $Vt_n = +0.7V$, $k'p = 42\ \mu A/V^2$, $V_{tp} = -0.8V$, and a power supply of $V_{DD} = 3.33V$ is used. Find mid point voltage VM if $(W/L)_n$=10 and $(W/L)_p = 14$. (8)

Or

(b) (i) Derive an equation for transconductance of an n-channel enhancement MOSFET operating in active region. (8)

(ii) Discuss the Switch model and Square law model of MOSFET. (8)

13. (a) Design and draw the CMOS circuits for the following function, use minimum number of transistor and assess the performance of the circuit. $F = XA + XY(A + B) + XYZ(A + B + C)$.

Or

(b) Design and analyze the performance of 4:1 MUX using CMOS and transmission gate logics.

14. (a) Use minimum no of transistor and implement the following logic in dynamic and domino logics. $W = abc + cde + efg$.

Or

(b) Develop a model of word line decoder delay for a RAM with $2n$ rows and $2m$ columns. Assume true and complementary inputs are available and that the input capacitance equals the capacitance of one of the columns of $H = 3m$. Use CMOS gates and express result in terms of n and m .

15. (a) Write a behavioural VHDL program for realizing an 8 bit shift register that could be configured to perform serial to parallel and parallel to serial shift logics.

Or

(b) (i) Draw the VHDL design flow model and explain the significance of each steps. (8)

(ii) Write a structural VHDL program for a 4 to 16 decoder circuit. (8)