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Question Paper Code : 51244

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Sixth Semester

Electronics and Communication Engineering

080290038 — VLSI DESIGN

(Common to Medical Electronics Engineering)

(Regulation 2008)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How does design rules classified?

2. Define Yield. What is the relation of yield with die area?

3. What is body bias? Obtain the threshold voltage equation with a body effect.

4. What is Latch-up in CMOS circuit? Mention the methods to prevent it.

5. Draw the layout of tristate inverter and give its significance.

6. How does transmission gates act as switch?

7. Sketch the logic diagram of clocked SR latch with its truth table.

8. Give the structure of dynamic RAM cell and write the impact of charge leakage from RAM cell.

9. What is the key difference between the variables and signals? Give example.

10. Design a 4:1 MUX using case statement.

PART B — (5 × 16 = 80 marks)

11. (a) (i) What is Photolithography? How does pattern transfer occurs in integrated circuits? (8)

    (ii) Discuss the SCMOS design rules used in N-well, contact and polyl regions. (8)

Or

    (b) Explain in detail the CMOS fabrication technique with neat diagram. (16)

12. (a) (i) Mention the operating regions of square law model and plot the V-I characteristics of nFET. (8)

    (ii) Explain the operation of nFET with its equation. (8)

Or

    (b) Derive the expression for MOSFET resistance and show all the parasitic capacitances of MOS transistor. (16)

13. (a) (i) Design a 2 to 4 decoder using

        (1) CMOS logic (4)

        (2) Transmission gates. (4)

    (ii) What is the purpose of cell libraries? Discuss the delay issues of cascaded inverter. (8)

Or

    (b) (i) What happens when CMOS inverters are connected in series? Obtain an expression to determined the time constant of the network. (8)

    (ii) Construct a logic diagram of half adder and use them as primitive in building a full adder circuit. (8)

14. (a) (i) Explain the operation of master-slave dynamic D Flip flop and construct a static clocked design out of dynamic D flip flop. (8)

    (ii) Give the operation of static RAM cell. (8)

Or

    (b) (i) Discuss the construction and working at dynamic logic gates and design a 2-input NAND using dynamic and domino logic. (10)

    (ii) Explain the operation of master-slave D-type Flip flop and show how the race condition is eliminated in it. (6)

15. (a) (i) Discuss the VHDL operators with an example. (8)

    (ii) Design a JK Flip flop using VHDL (8)

Or

(b) (i) Write the VHDL code for a 4-bit full adder using structural modelling. (8)

    (ii) Develop a VHDL code for the following state table using behavioral modelling. (8)

PS		NS		O/P
y_1	y_2	y_1	$y_2 Z$	
		$x = 0$	$x = 1$	
0	0	00, 0	10, 0	
0	1	00, 0	11, 0	
1	0	10, 0	01, 0	
1	1	10, 0	11, 1	

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