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Question Paper Code : 60464

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Sixth Semester

Electronics and Communication Engineering

EC 2354/EC 64 — VLSI DESIGN

(Regulations 2008)

(Common to PTEC 2354 – VLSI Design for B.E. (Part-Time) Fifth Semester – Electronics and Communication Engineering – Regulations 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the various issues in Technology-CAD.

2. Define the lambda layout rules.

3. Give the effect of supply voltage and temperature variations on the CMOS system performance.

4. What are the factors that cause static power dissipation in CMOS circuits?

5. Implement a 2:1 Multiplexer using pass transistor.

6. Design a 1-bit dynamic register using pass transistor.

7. What is a Tester, Test Fixture and Handler?

8. Mention the different types of CMOS testing techniques.

9. What are procedural assignments in Verilog?

10. What is a switch level modeling?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the different steps involved in n-well CMOS fabrication process with neat diagrams. (10)

(ii) Draw the CMOS inverter and discuss its DC characteristics. Write the conditions for the different regions of operation. (6)

Or

(b) (i) An NMOS transistor has a nominal threshold voltage of 0.16 V. Determine the shift in threshold voltage caused by body effect using the following data. The nMOS transistor is operating at a temperature of 300°K with the following parameters : gate oxide thickness $(t_{OX}) = 0.2 \times 10^{-5}$ cm, relative permittivity of gate oxide $(\varepsilon_{OX}) = 3.9$, relative permittivity of silicon $(\varepsilon_{Si}) = 11.7$, substrate bias voltage = 2.5 V, intrinsic electron concentration $(N_i) = 1.5 \times 10^{10} / \text{cm}^3$, impurity concentration in substrate $(N_A) = 3 \times 10^{16} / \text{cm}^3$. Given Boltzmann's constant = 1.38×10^{-23} J/°K, electron charge = 1.6×10^{-19} Coulomb and permittivity of free space = 8.85×10^{-14} F/cm. (8)

(ii) Explain the principle of SOI technology with neat diagrams. Discuss its advantages and disadvantages. (8)

12. (a) Derive an expression for the rise time, fall time and propagation delay of a CMOS inverter.

Or

(b) Explain the various ways to minimize the static and dynamic power dissipation.

13. (a) Explain in detail about the pipeline concepts used in sequential circuits. (16)

Or

(b) Discuss the design techniques to reduce switching activity in a static and dynamic CMOS circuits, (16)

14. (a) (i) List the manufacturing test principles and explain them. (8)

(ii) Explain Built-in Self-Test. (8)

Or

(b) (i) Discuss on the Test Logic Architecture and Test Access Port. (8)

(ii) Explain on the scan design strategy of testing. (8)

15. (a) Explain the following in VERILOG with an suitable example : (16)

(i) Timing controls and Conditional statements

(ii) Behavioural and Gate level modelling.

Or

(b) Write the VERILOG code for (16)

(i) Priority Encoder

(ii) Equality Detector.

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