Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 31268

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2013.

18.5.13.FN

Sixth Semester

Electronics and Communication Engineering

080290038 — VLSI DESIGN

(Common to Medical Electronics Engineering)

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Specify any two techniques and processes involved in Photolithography.
2. How can you define the layout design rules?
3. Draw the diagram for SPICE MOSFET model.
4. How do you construct the Voltage Transfer Curve for a CMOS Inverter?
5. Construct a Complex CMOS gate for $OUT = \overline{D + A.(B + C)}$.
6. What are the advantages of Cell libraries in CMOS?
7. What is meant by Domino Gates?
8. Draw a SR latch using NOR gates and Construct the characteristics and excitation table.
9. What are the advantages of VHDL?
10. What are the various operators used in VHDL?

PART B — ($5 \times 16 = 80$ marks)

11. (a) (i) Explain the various steps involved in fabrication of N-Channel MOSFET. (8)

(ii) Explain about the working principle of n-MOS enhancement Transistor with various modes of operation. (8)

Or

(b) Explain in detail the functions of CMOS design rule set for different layers. (16)

12. (a) (i) What do you mean by CMOS Latch up? How can you handle the Latch up problem in CMOS circuits. (8)

(ii) Discuss about the MOSFET operation in detail. (8)

Or

(b) Write a technical note on the following

(i) Propagation delay of CMOS Inverter (4)

(ii) Estimation of the Load Capacitance (4)

(iii) Noise Margin (4)

(iv) Calculation of Parasitic Depletion Capacitance. (4)

13. (a) (i) Draw the Stick diagram for CMOS NOR Gate and NAND gate. (8)

(ii) Design CMOS logic circuits for the following function: (8)

$$Z = \overline{(A.B)+C.(A+B)}$$

Or

(b) (i) Discuss some of the standard Cell libraries used in CMOS process in VLSI design. (6)

(ii) With neat schematic diagram and truth table, Explain about the operation of Transmission Gate and Pass Transistor logic circuit. (10)

14. (a) Explain briefly about the following:

(i) D Type flip flop operation with truth table (4)

(ii) Classical positive-edge-triggered D flip-flop (4)

(iii) Master—slave pulse-triggered D flip-flop (4)

(iv) Edge-triggered dynamic D storage element. (4)

Or

(b) (i) State and Compare Static logic and Dynamic Logic. (8)

(ii) Discuss about basic operations of dynamic memories. (8)

15. (a) (i) Write a structural VHDL code for JK flip flop. (8)

(ii) Write a VHDL code to design a 4-bit Adder using VHDL description of combinational network. (8)

Or

(b) (i) Explain the VHDL design flow model in detail. (8)

(ii) Write a VHDL code for binary counter using data flow modeling. (8)
