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Question Paper Code : 51414

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2014.

Sixth Semester

Electronics and Communication Engineering

EC 2354/EC 64/10144 EC 704 — VLSI DESIGN

(Regulation 2008/2010)

(Common to PTEC 2354 – VLSI Design for B.E. (Part – Time) Fifth Semester – Electronics and Communication Engineering – Regulation 2009)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the non-ideal I-V effects?
2. Discuss any two layout design rules.
3. Define Transistor sizing problem.
4. What do you mean by design margin.
5. What are synchronizers?
6. State any two criteria for low power logic design?
7. What is the need for testing?
8. What do you mean by Text Fixtures?
9. What are procedural assignments in Verilog?
10. What is a switch level modeling?

PART B — (5 × 16 = 80 marks)

11. (a) Discuss the CV characteristics and DC transfer characteristics of the CMOS. (16)

Or

(b) Briefly discuss about the CMOS process enhancements and layout design rules.

12. (a) Explain the following,

(i) Device models and device characterizations. (10)

(ii) Power dissipation in CMOS circuits. (6)

Or

(b) (i) Describe the simulation of circuit Interconnects. (8)

(ii) Write about SPICE based circuit simulation. (8)

13. (a) Explain the methodology of sequential circuit design of Latches and Filpflops. (16)

Or

(b) Briefly discuss about the classification of circuit families and comparison of the circuit families. (16)

14. (a) Discuss the need for testing and explain about the silicon debugging principles. (16)

Or

(b) Explain the method of boundary scan test in detail. (16)

15. (a) Explain the following in VERILOG with an suitable example.

(i) Timing controls and Conditional Statements

(ii) Behavioural and Gate level Modelling. (16)

Or

(b) Write the VERILOG code for

(i) Priority Encoder

(ii) Equality Detector. (16)
