Reg. No. | | | | | | | | | | | | |

Question Paper Code : 57297

B.E/B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Sixth Semester

MEDICAL ELECTRONICS

EC 6601 – VLSI DESIGN

(Common to Electronics and Communication Engineering

(Regulations 2013)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. State channel-length modulation. Write down the equation for describing the channel length modulation effect in NMOS transistors.
2. What is Latch-up ? How to prevent latch up ?
3. Give Elmore delay expression for propagation delay of an inverter.
4. Why single phase dynamic logic structure cannot be cascaded ? Justify.
5. Draw the switch level schematic of multiplexer based nMOS latch using nMOS only pass transistors for multiplexers.
6. What is clocked CMOS register ?
7. What is meant by bit-sliced data path organization ?
8. Determine propagation delay of n-bit carry select adder.
9. What are feed-through cells ? State their uses.
10. State the features of full custom design.

PART – B (5 × 16 = 80 Marks)

11. (a) (i) Describe the equation for source to drain current in the three regions of operation of a MOS transistor and draw the VI characteristics. (8)

(ii) Explain in detail about the body effect and its effect in MOS device. (8)

OR

(b) (i) Explain the DC transfer characteristics of a CMOS Inverter with necessary conditions for the different regions of operation. (8)

(ii) Discuss the principles of constant field and lateral scaling. Write the effects of the above scaling methods on the device characteristics. (8)

12. (a) (i) Draw the static CMOS logic circuit for the following expression (8)

(a) $Y = \left(\overline{A \cdot B \cdot C \cdot D}\right)$

(b) $Y = \overline{D(A + BC)}$

(ii) Discuss in detail the characteristics of CMOS transmission gate ? (8)

OR

(b) What are the sources of power dissipation in CMOS and discuss various design techniques to reduce power dissipation in CMOS ? (16)

13. (a) Explain the operation of master-slave based edge triggered register. (16)

OR

(b) Discuss in detail various pipelining approaches to optimize sequential circuits. (16)

14. (a) Design a 16 bit carry bypass and carry select adder and discuss their features. (8 + 8)

OR

(b) Design a 4 × 4 array multiplier and write down the equation for delay. (16)

15. (a) With neat sketch explain the CLB, IOB and programmable interconnects of an FPGA device. (16)

OR

(b) Write brief notes on :

(a) Full custom ASIC (8)

(b) Semi custom ASIC (8)
