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Question Paper Code : 11269

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2014.

Sixth Semester

Electronics and Communication Engineering

080290038 — VLSI DESIGN

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. List the different steps in CMOS fabrication.
2. What are Contact Cuts and Via?
3. Define Figure of Merit of a MOS transistor.
4. What is latch up problem in CMOS circuits?
5. State the differences between Transmission Gate and Pass Transistor.
6. List the importance features of standard cell design.
7. What is Domino logic?
8. State the advantages of two-phase clocking in clocked sequential circuits.
9. What is an entity in VHDL?
10. Differentiate between concurrent and sequential codes.

PART B — ($5 \times 16 = 80$ marks)

11. (a) (i) Explain with a neat diagram the n-well CMOS process of fabrication highlighting the steps involved. (8)

(ii) Explain the different types of Contact Cuts between polysilicon and diffusion layer in nMOS circuits along with their dimensional details. (8)

Or

(b) (i) Describe the steps involved in nMOS transistor fabrication process. Illustrate with neat diagrams the steps involved. (8)

(ii) Explain the λ based transistor design rules for nMOS and CMOS transistors. (8)

12. (a) (i) Derive the expression for drain current and threshold voltage for a nMOS transistor structure alone with its characteristics diagram. (8)

(ii) Explain how latch up problems are overcome in CMOS circuits. (8)

Or

(b) (i) Explain the parasitic capacitances associated in the nMOS transistor circuit model. (8)

(ii) Determine the pull-up to pull-down ratio for an nMOS inverter driven through one or more pass transistor. (8)

13. (a) (i) Draw the stick diagrams of the NAND and NOR circuits using CMOS. (8)

(ii) Explain the operations of transmission gate and pass transistor along with their layout diagrams. (8)

Or

(b) (i) With an example, explain the construction of Euler graph. (8)

(ii) Describe the method of extension of a layout technique to a complex logic Gate. (8)

14. (a) (i) With a neat layout diagram explain the static RAM 6T cell and its writing and reading operations. (8)

(ii) Describe the central SRAM block architecture along with the operation of the row driver circuit. (8)

Or

(b) (i) With the diagram explain the write and hold operations of a 1T DRAM cell How is refresh operation carried out in a DRAM cell. (8)

(ii) Explain the operation of a non-inverting domino logic gate along with its layout. (8)

15. (a) Write short notes on the following :

(i) Design hierarchies. (8)

(ii) Architecture module in VHDL. (8)

Or

(b) Write a VHDL program for a 8 bit shift register using structural modeling.
