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Question Paper Code : 40936

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2018
Seventh Semester
Electronics and Communication Engineering
EC 6009 – ADVANCED COMPUTER ARCHITECTURE
(Regulations 2013)

Time : Three Hours   Maximum : 100 Marks

Answer ALL questions

PART – A   (10×2=20 Marks)

1. Define throughput.

2. Some microprocessors today are designed to have adjustable voltage, so that a 15% reduction in voltage may result in a 15% reduction in frequency. What would be the impact on dynamic power ?

3. What is pipelining ?

4. Outline the limitations of instruction level parallelism.

5. Define data-level parallelism.

6. What is SIMD ?

7. Define a process and a thread.

8. What is a chip multiprocessor ?

9. Outline the difference between volatile memory and non-volatile memory.

10. Define cache hit and cache miss.

PART – B   (5×16=80 Marks)

11. a) Appraise the major factors that influence the cost of a computer and outline how these factors are changing over time.   (16)

(OR)

b) i) Appraise module reliability and module availability with an example.   (8)

ii) How to relate the performance of two different computers, say, X and Y ? Appraise with an example.   (8)

12. a) Appraise with an example the use of simple compiler technology to enhance a processor's ability to exploit instruction level parallelism. **(16)**

        (OR)

    b) How data hazards can be overcome with dynamic scheduling ? Appraise with an example. **(16)**

13. a) Explain with a diagram the basic structure of a vector processor. **(16)**

        (OR)

    b) i) Present an outline of graphical processing units. **(8)**

       ii) Explain loop level parallelism with an example. **(8)**

14. a) i) What is a multiprocessor ? Explain with a diagram the basic structure of a symmetric shared-memory multiprocessor. **(8)**

       ii) Explain how to implement synchronization in a multiprocessor using a set of hardware primitives with the ability to atomically read and modify a memory location. **(8)**

        (OR)

    b) Explain with an example sequential consistency model and relaxed consistency model for memory consistency. **(16)**

15. a) Explain with an example any two techniques for improving the cache performance by reducing the miss rate. **(16)**

        (OR)

    b) What is RAID ? Explain the different levels of RAID. **(16)**

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