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Question Paper Code : X 10352

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020

Third Semester

Electronics and Communication Engineering

EC 8351 – ELECTRONIC CIRCUITS – I

(Common to Electronics and Telecommunication Engineering)

(Regulations 2017)

Time : Three Hours

Maximum : 100 Marks

Answer ALL questions

PART – A

(10×2=20 Marks)

1. Why self biasing is better than fixed biasing ?
2. What are Q-point and load line of transistor circuits ?
3. Compare CE, CB and CC configurations of BJT amplifiers.
4. Define CMRR.
5. Draw small signal hybrid pi equivalent circuit of MOSFET.
6. Where BiCMOS circuits are used ?
7. Why the gain of amplifiers are lower at low frequencies and high frequencies ?
8. Draw the typical frequency response curve of RC-coupled CE BJT amplifier and label upper cut-off, lower cut-off frequencies and bandwidth.
9. Draw the block diagram of a regulated DC power supply.
10. Define ripple factor and rectification efficiency.

PART – B

(5×13=65 Marks)

11. a) Define stability factor for leakage current and derive its general expression. Derive the expression for stability factor for leakage current of emitter stabilized biasing circuit.

(OR)

- b) An npn BJT amplifier is provided with potential divider biasing. The Q points are $I_C = 1 \text{ mA}$ and $V_{CE} = 5\text{V}$. Given $V_{CC} = 20\text{V}$, $V_{RE} = 3\text{V}$, $\beta = 100$ and $V_{BE} = 0.6\text{V}$. For a stability factor of 5, design the bias circuit.



12. a) For a common emitter (emitter bypassed) amplifier, $V_{CC} = 9V$, $R_E = 1.2 \text{ k}\Omega$, $R_1 = 27 \text{ k}\Omega$, $R_2 = 15 \text{ k}\Omega$, $R_s = 10 \text{ k}\Omega$, $R_L = 2 \text{ k}\Omega$, $R_C = 2.2 \text{ k}\Omega$. If $\beta = 100$, $V_{BE} = 0.7 \text{ V}$ and $V_A = 100V$, determine input resistance, output resistance, voltage gain and current gain. Also determine the voltage gain by taking source resistance into consideration.

(OR)

- b) Using hybrid π model, obtain the expression for input impedance, output impedance and mid band voltage gain of a common emitter amplifier.
13. a) Draw the circuit of a common source amplifier using MOSFET. Derive the expressions for voltage gain and input resistance.

(OR)

- b) Derive expression for voltage gain, input impedance and output impedance of enhancement MOSFET drain feedback configuration.
14. a) Make a detailed note on frequency response of RC coupled amplifier. Also discuss the effects of circuit capacitors and internal capacitances on the frequency response.

(OR)

- b) Write short notes on :
- i) Miller effect capacitance. (5)
 - ii) Cut off frequency. (4)
 - iii) Unity gain bandwidth. (4)
15. a) Draw the circuit of a series voltage regulator and explain its operation. Discuss how short circuit protection can be provided in the circuit.

(OR)

- b) i) Compare half-wave rectifier power supply and full-wave rectifier power supply on the basis of different performance metrics. (7)
- ii) Discuss about SMPS with necessary diagrams. (6)



PART – C

(1×15=15 Marks)

16. a)

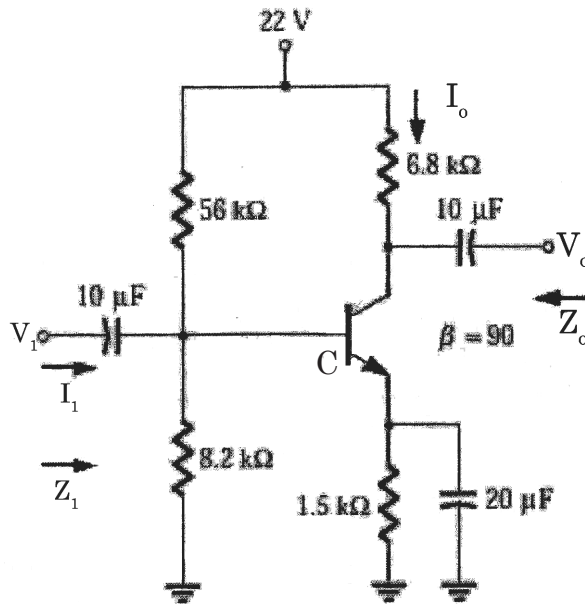


Fig. 1

For the common emitter network shown in Fig. 1, determine :

- a) r_e
- b) Z_i
- c) Z_o ($r_o = \infty$)
- d) A_v ($r_o = \infty$)
- e) A_i ($r_o = \infty$).

(OR)

- b) i) Explain ac and dc load lines with necessary schematics. (10)
- ii) Given the load line in Fig. 2 and the defined Q-point, determine the required values of V_{CC} , R_C , and R_B for a fixed-bias configuration. (5)

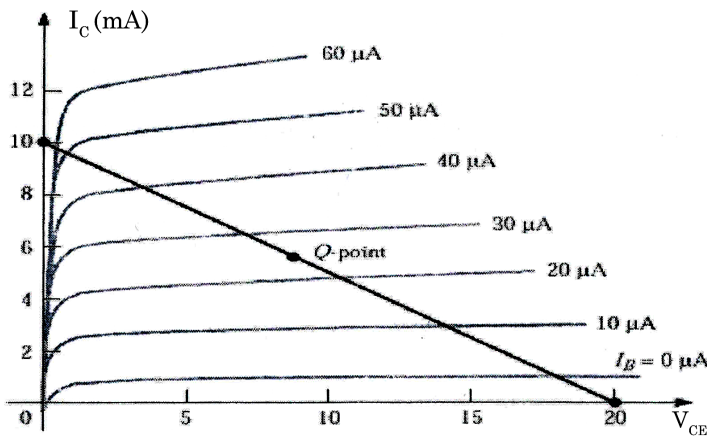


Fig. 2