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Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 80115

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Third/Fourth Semester

Electronics and Communication Engineering

EC 8392 — DIGITAL ELECTRONICS

(Common to Medical Electronics/Biomedical Engineering/Computer and Communication Engineering/Mechatronics Engineering/Robotics and Automation Engineering)

(Regulation 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. What is the largest binary number that can be expressed with 14 bits? Determine the equivalent decimal and hexadecimal numbers.

2. Find the complement of $F = wx + yz$ and then show that $FF' = 0$.

3. Draw the truth table for a half adder circuit and write the Boolean expressions for sum and carry.

4. What is meant by a decoder circuit?

5. Draw the logic diagram and function table of a SR latch implemented using NAND gates.

6. How many flipflops will be complemented in a 10-bit ripple counter to reach the next count after this count of '1001100111'?

7. Define a "flow table".

8. Distinguish between non-critical face and critical race.

9. A DRAM ship uses two dimensional address multiplexing. It has 13 common address pins with the row address having one bit more than the column address. What is the capacity of the memory?

10. A standard TTL gate has the following current specifications :

$I_{OH} = 400\ \mu A$, $I_{IH} = 40\ \mu A$, $I_{OL} = 16\ mA$, $I_{IH} = 1.6\ mA$. Calculate the fanout.

PART B — (5 × 13 = 65 marks)

11. (a) Use Karnaugh map method to simplify the following Boolean function

$F(A, B, C, D) = \sum m\,(2, 4, 6, 10, 12) + d(0, 8, 9, 13)$

Implement the Boolean function, F using not more than two NOR gates.

Or

(b) Implement the following function using Quine McCluskey method

$F = \sum m\,(6, 7, 8, 9) + d\,(10, 11, 12, 13, 14, 15)$

12. (a) With a neat diagram, explain the working of a four bit adder-subtractor circuit.

Or

(b) With a truth table and logic diagram, explain the operation of a four input priority encoder.

13. (a) Draw the neat diagram of a 4-bit universal shift register and explain it's operation.

Or

(b) A sequential circuit has two JK flip-flops A and B , two inputs x and y and one output z. The flip-flop input equations and circuit output equation are:

$J_A = Bx + B'Y'$ $\qquad$ $J_B = A'x$

$K_A = B'xy'$ $\qquad$ $K_B = A + xy'$ $\qquad$ $z = Axy + Bx'Y'$

Draw the logic diagram and state table of the circuit. Also derive the state equations for A and B.

14. (a) An asynchronous sequential circuit is described by the excitation function, $Y = x_1x_2' + (x_1 + x_2')\,y$ and the output function $z = y$. Draw the logic diagram of the circuit. Derive the transition table and output map. Also discuss about the behavior of the circuit.

Or

(b) Briefly explain about race-free state assignment with relevant examples.

15. (a) Implement the full adder circuit using PLA by deriving the PLA programming table.

Or

(b) Explain about the tri-state TTL output configuration with a neat diagram.

PART C — (1 × 15 = 15 marks)

16. (a) Derive the ROM programming table for the combinational circuit that squares a 4-bit number. Minimize the number of product terms.

Or

(b) Design a counter with T flip-flops that goes through the following binary repeated sequence 0,1,3,7,6,4. Show that when binary states 010 and 101 are taken to be don't care conditions, the counter may not operate properly. Find a way to correct the design.

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