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Question Paper Code : X 10367

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Fifth Semester
Electronics and Communication Engineering
EC 8552 – COMPUTER ARCHITECTURE AND ORGANIZATION
(Common to Electronics and Telecommunication Engineering)
(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. What is the impact of frequency of clock signal applied to the microprocessor in the performance of computers ?

2. Identify the addressing mode involved in the instruction XOR R1, [R2 + 100], R1 and determine the resultant stored in register R1 if all of its bit were 1's initially. (Assume three address instruction format in which the first two operands are source and the last one is the destination)

3. Draw the circuit schematic of a bit-cell using primitive gates that implements carry generate and propagate signals along with the sum bit of a pairwise inputs and carry signal from the preceding stage.

4. What is the meaning of biased exponent ? State the values of bias in the IEEE 754-1985 single and double precision formats, respectively.

5. State the purpose of the following registers in processor architectures : PC, MDR, IR and MAR.

6. State whether the instruction sequence MUL R3, R1, R2 and SUB R2, R3, R1 in succession when executed using a four stage pipelined processor will result in hazard or not. Justify.

7. What is the purpose of tag field in addressing a cache memory ? Assuming that processor generates 16 bit address and that the cache memory is organized as a 64 blocks of 16 words in every block, estimate the number of bits required for the tag field.

8. What is baud rate ? Is this term associated with serial or parallel communication standard ?

9. What are the types of hardware multithreading ? How does SMT differ from these types ?

10. Differentiate : GPUs and CPUs.

PART – B **(5×13=65 Marks)**

11. a) i) How are the generations of computers classified ? Give an overview of evolution of computer architectures from the first to the present generation. **(8)**

ii) Give a general expression to evaluate performance of a computer in terms of the number of instructions, operations and the clock frequency. Suggest a few architectural features using which this performance metric could be improved upon. **(5)**

(OR)

b) i) What is zero address instruction format ? Give an example. **(3)**

ii) Enumerate the most commonly used addressing modes of CPU instructions. **(6)**

iii) Registers R1 and R2 of a computer contain the decimal values 1200 and 4600. what is the effective address of the memory operand of the following instruction : Load 25(R1), R5. **(4)**

12. a) i) Show that the subtraction of an n-bit subtrahend from an n-bit minuend could be performed by addition operation with a suitable example. **(6)**

ii) State the purpose of Look Ahead Carry Adder. Derive the expressions for propagate and generate functions of a 4-bit Look Ahead Carry Adder and draw its schematic. **(7)**

(OR)

b) i) Consider a 32-bit floating point representation number system. What are the regions in which the numbers are not included in the range of numbers in such representation ? **(6)**

ii) Perform multiplication of integers 14 and –7 using Booth's multiplication algorithm. **(7)**

13. a) i) Explain the internal organization of a single-bus processor with a neat sketch showing the internal bus connecting the building blocks. **(8)**

ii) Distinguish between the visible and invisible registers available in processor organizations with specific examples. **(5)**

(OR)

b) i) Show that a five stage pipelined architecture would achieve a considerable saving on the execution time over that of a non-pipelined architecture with a neat sketch of timing diagram. Assume that all the stages viz. OF, ID, OR, EX and OW spend one unit of time for all the instructions. Determine the speed up achievable by the pipelined architecture in the absence of hazards of any types. **(8)**

ii) List the types of hazards and briefly explain the impact of such hazards on the performance of the pipelines. **(5)**

14. a) i) How does a DRAM differ from that of SRAM ? State the need for the refresh logic in DRAMs. **(5)**

ii) In a hierarchical memory system, where does the cache memory placed ? Explain the terms 'locality of reference' and 'cache line'. **(8)**

(OR)

b) i) Distinguish between the strobed I/O and interrupt driven data transfer modes. **(5)**

ii) What is the use of Translation Lookaside Buffers in Virtual Memory organization ? With a neat sketch explain the organization of associative-mapped TLB. **(8)**

15. a) i) Classify the computer architectures according to the Flynns taxonomy and write a brief note on level of parallelism achievable on these types of architectures. **(6)**

ii) Write detailed notes on Multiprocessor Network Topologies. **(7)**

(OR)

b) i) Explain the concept of cluster architecture with Google Server as an example. **(6)**

ii) Enumerate the types of network topologies and depict all such topologies pictorially for the interconnection of 8 nodes. **(7)**

PART – C **(1×15=15 Marks)**

16. a) i) Consider the following analogy of the concept of caching : A serviceman visits a house for a repair work. He uses the tools in the toolbox that he carried until he is in need of a tool which is not in the box. There is a chance that the required tool is available in the vehicle that he came from his office; if not he has to go to his office to bring the required tool to complete the work.

Suppose we argue that the toolbox, the vehicle and the office resemble that of L1, L2 cache and main memories of a computer, respectively. Is this a correct analogy ? Discuss its correct or incorrect features. **(8)**

ii) A disk unit has 24 recording surfaces. It has a total of 14,000 cylinders. There is an average of 400 sectors per track. Each sector contains 512 bytes of data. Determine the data transfer rate in bytessec at a rotational speed of 7200 rpm. Using a 32-bit word, suggest a suitable scheme for specifying the disk address, assuming that there are 512 bytes per sector. **(7)**

(OR)

b) Assume that a processor has 24-bit address bus and 8-bit data bus. Design a computer system that interfaces this processor with RAM of size 512 KB made of 64 KB chips and 64 KB of single chip ROM with address map starting at locations 400000 and 000000 respectively. Draw a neat sketch of the schematic diagram showing the interconnections and the address decoder. **(15)**

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