23/12/23 - AN

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 70518

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2023.

Fifth Semester

Electronics and Communication Engineering

EC 8552 – COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Electronics and Telecommunication Engineering)

(Regulations 2017)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Differentiate execution time and throughput.
2. List the uses of instruction register and program counter.
3. State the two ways detect overflow in an n-bit adder.
4. Give an example for the worst case of Booth's algorithm.
5. What are the major characteristics of a pipeline?
6. Differentiate imprecise and precise exception.
7. Can IO devices be connected directly to the system bus? Give reasons.
8. Define data stripping.
9. Name two methods of achieving parallelism.
10. Compare warehouse scale computers with data centers.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Differentiate shared memory multiprocessors and distributed memory multi computers. (8)

(ii) Explain how performances gain is calculated using Amdahl's law. (5)

Or

(b) (i) Explain the Flynn's classification of computer architecture. (8)

(ii) How is register direct addressing mode different from register indirect addressing mode? (5)

12. (a) (i) List the steps for performing restoring division and non-restoring division. (8)

(ii) State the advantages of non-restoring over restoring division. (5)

Or

(b) (i) Explain floating point representation with an example. (8)

(ii) Name the 2 IEEE standards for the floating point numbers. (5)

13. (a) With diagrams, explain the pipelined execution of successive instructions in a base scalar processor and in two under pipelined cases. (13)

Or

(b) Explain how data hazards are overcome by dynamic scheduling using Tomasulo's algorithm. (13)

14. (a) (i) Explain various techniques used for the reduction of miss penalty and miss rate. (7)

(ii) Discuss the protection mechanism used for virtual memory. (6)

Or

(b) (i) Explain the three types of internal communication methodologies. (7)

(ii) Write short notes on RAID structure. (6)

15. (a) (i) List the challenges of parallel processing architecture. (7)

(ii) Illustrate the concept of Hardware multithreading. (6)

Or

(b) Explain the classification of multiprocessor network topologies based on their topological properties. (13)

PART C — (1 × 15 = 15 marks)

16. (a) (i) With state diagrams, explain the transition diagram for a pipeline unit. (8)

(ii) Explain the pipelined execution for the given instructions : (7)

- $X = Y + Z$
- $A = B \times C$

Or

(b) (i) With a flowchart, explain the algorithm for performing floating point multiplication. (7)

(ii) Differentiate cache memory and virtual memory. (8)

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