5/6/23 AN

Reg. No.: | | | | | | | | | | | | |

Question Paper Code : 50477

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2023.

Sixth/Seventh Semester

Electronics and Communication Engineering

EC 8095 – VLSI DESIGN

(Common to: Electrical and Electronics Engineering/ Electronics and Instrumentation Engineering/Electronics and Telecommunication Engineering/Instrumentation and Control Engineering/Robotics and Automation)

(Regulations – 2017)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How CMOS acts as a switch?
2. What is the Elmore delay for 4-input NAND gate?
3. List the advantages and disadvantages of pass transistor logic.
4. Realize the 2:1 multiplexer using transmission gates.
5. Differentiate monostability and astability sequential circuits.
6. Differentiate latches and flipflops.
7. What are the basic building blocks of digital architectures?
8. Write the steps for single bit addition.
9. What is routing?
10. State the need for testing.

PART B — (5 × 13 = 65 marks)

11. (a) Illustrate the long channel I-V and C-V characteristics of MOS transistor. (13)

Or

(b) Explain the DC transfer characteristics of MOS transistor. (13)

12. (a) Describe the operation of dynamic CMOS logic. Discuss the charge-sharing problem in dynamic CMOS logic and provide the solution to overcome the charge-sharing problem. (13)

Or

(b) (i) Elucidate the Cascode voltage switch logic with a suitable example. (6)

(ii) Show how static power and dynamic power are dissipated in CMOS circuits. (7)

13. (a) (i) What is pipelining? Explain the concept of pipelining in sequential circuits with a suitable example. (7)

(ii) Elucidate the sense amplifier based register? (6)

Or

(b) (i) What is synchronous design? Identify and explain the timing issues in synchronous design. (7)

(i) Illustrate the astability sequential circuits using MOS transistor. (6)

14. (a) Describe the operation of Carry Bypass adders and find the worst case path delay. (13)

Or

(b) (i) Examine the working of SRAM using CMOS logic. (6)

(ii) Draw the DRAM sub-array and open bit lines architecture for processing. (7)

15. (a) Examine the boundary scan architectures and show how to test the system level architectures. (13)

Or

(b) (i) Elucidate the basic types of programmable elements of FPGA. (6)

(ii) Compare any two types of Ad hoc scanning methods with suitable example. (7)

PART C — (1 × 15 = 15 marks)

16. (a) Realize the function Y= (AC'+BD)' using (i) Ratioed logic (ii) CMOs logic (iii) Dynamic logic (iv) Domino logic (v) Pass transistor logic. (3+3+3+3+3)

Or

(b) Elucidate the Master-Slave Edge-Triggered register? Analyze the timing properties for Non-ideal clock signals. (15)
