Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 82143

M.E. DEGREE EXAMINATION, JUNE 2012.

Elective

VLSI Design

VL 9261/252079/AP 954/10244 VLE 11 — ASIC DESIGN

(Common to M.E Applie ¡ Electronics/M.E Computer and Communication and M.E. Electronics and Communication Engineering)

(Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Draw the ASIC Design flow.
2. Mention the various parasitic capacitance assosiated with the CMOS transistors.
3. Illustrate the operation of antifuses and give their types.
4. What is short circuit power dissipation?
5. Distinguish between Altera 5000 and 7000.
6. Expand EDIF and illustrate the hierarchical nature of an EDIF file.
7. State the difference between the logic synthesis and simulation.
8. What is an fault simulation? What are the various types of fault simulation?
9. Define Connectivity matrix.
10. Differentiate Pad limited and Core limited die.

PART B — ($5 \times 16 = 80$ marks)

11. (a) (i) Explain the different types of ASIC with neat diagram. (11)
(ii) Mention the features need for an ASIC cell library. (5)

Or

(b) Explain about the Combinational and Sequential logic cell design in ASIC. (16)

12. (a) Explain about the various programming technologies used for programmable ASICS. (16)

Or

(b) Describe about the DC and AC input I/O requirements for the ASICs. (16)

13. (a) (i) With a neat diagram, explain Xilinx LCA interconnect. (8)

(ii) Discuss about schematic entry and Logical Synthesis. (8)

Or

(b) (i) With a neat sketch, explain Actel ACT interconnect. (8)

(ii) Dereive from the first principle an expression for RC delay in antifuse. (8)

14. (a) Describe the ATPG algorithm in detail with an example and a method to validate the test pattern. (16)

Or

(b) Discuss in detail about the various combinational and sequential statements used in VHDL using suitable example. (16)

15. (a) (i) Briefly explain the K-L algorithm with a suitable example. (12)

(ii) Explain in detail about the FPGA partitioning. (4)

Or

(b) (i) With diagrams, show the channel routing orders for a slicing floorplan. (10)

(ii) Explain global routing with necessary diagrams. (6)

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