Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 82450

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Elective

VLSI Design

VL 9261/AP 954/UAP 9167/10244 VLE 11 — ASIC DESIGN

(Common to M.E. – Digital Communications and Networking/M.E. Applied Electronics, M.E. Computer and Communication and M.E. Electronics and Communication Engineering)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Differentiate between Full custom and Standard cell based ASICs.

2. Define logical effort of a logic cell.

3. List the PREP benchmarks

4. Give any two differences between Altera Flex and Altera MAX.

5. Define Elmore's constant

6. What is logic synthesis?

7. What is the use of architecture in VHDL?

8. List the four basic steps in PODEM algorithm

9. What are the three steps for min-cut placement method?

10. Differentiate between Global routing and Detailed routing.

PART B — (5 × 16 = 80 marks)

11. (a) (i) With a neat flow chart, explain ASIC design flow. (8)

(ii) Explain the CMOS design rules with relevant diagrams. (8)

Or

(b) (i) Discuss in detail the parasitic capacitances associated for a n-channel MOSFET along with its diagram. (8)

(ii) Explain logical area and logical efficiency with an example of a single stage OR-AND-INVERT cell. (8)

12. (a) (i) Explain the poly-diffusion antifuse along with its diagram. (8)

(ii) Explain the Actel ACT 1 logic module as a Boolean Function generator. (8)

Or

(b) (i) Describe the logic expanders with simple diagrams. (8)

(ii) With a graphical representation of CMOS logic thresholds, explain the characteristics of CMOS inverter in switching between low and high thresholds. (8)

13. (a) (i) With neat diagrams, explain the interconnect architecture of Actel ACT family FPGA. (8)

(ii) Derive the generalized RC delay expression in antifuse connections. (8)

Or

(b) (i) Explain on Xilinx LCA interconnect architecture. (8)

(ii) Discuss the Netlist screener. (8)

14. (a) Write a VDHL program for the following :

(i) JK master slave Flip Flop. (8)

(ii) Four bit serial in and serial out register. (8)

Or

(b) (i) Describe the Boundary scan test. (8)

(ii) List the steps involved in the ATPG algorithm. (8)

15. Write short notes on the following :

(a) (i) Ratio-Cut algorithm for partitioning. (8)

(ii) Iterative placement improvement. (8)

Or

(b) (i) Detailed Routing. (8)

(ii) Circuit extraction. (8)
