Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 11924

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Elective

VLSI Design

VL 9261/AP 954/UAP 9167/10244 VLE 11 — ASIC DESIGN

(Common to M.E. Digital Communication and Networking/ M.E. Electronics and Communication/ M.E. Computer and Communication/M.E. Applied Electronics)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define structure gate array.
2. What is meant by full custom ASIC's?
3. What are the advantages of a metal metal antifuse over a poly diffusion antifuse?
4. What is the difference between EEPROM and EPROM technologies?
5. What is BIDI?
6. Define schematic entry.
7. Differentiate between physical faults and logical faults.
8. What is functional simulation?
9. What are the objectives of system partitioning?
10. Define channel definition.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the sequence of steps to design an ASIC. (9)

(ii) Explain the design rules of CMOS process with neat diagram. (7)

Or

(b) (i) Construct data path logic of 6 bit array multiplier using different data path. (9)

(ii) Explain the components of transistor parasitic capacitance. (7)

12. (a) (i) Explain the various ways to terminate transmission lines in programmable ASIC I/O cells. (8)

(ii) Discuss in detail about XILINX input/output block. (8)

Or

(b) (i) Explain PREP bench mark circuits to choose suitable FPGA. (8)

(ii) With a block diagram, explain the architecture of ALTERA flex cell. (8)

13. (a) (i) Describe the interconnect architecture used in an Actel ACT. (8)

(ii) Explain the most common method of design entry for ASIC's, (8)

Or

(b) (i) Explain the schematic design entry for ASIC with a suitable example. (8)

(ii) Discuss the various PLA tools for logic minimization in ASIC's. (8)

14. (a) (i) Write a VHDL program for a positive edge triggered D-flip-flop. (10)

(ii) Explain the various data types and wire type in Verilog. (6)

Or

(b) (i) Explain the gate level simulation and structural simulation for VHDL model.

(ii) Explain the Boundary scan test for ASIC's.

15. (a) (i) Explain the various sources of power dissipation in CMOS logic. (8)

(ii) Explain the different methods of partitioning with neat diagram. (8)

Or

(b) (i) Discuss the Floor planning tools for cell based ASIC. (8)

(ii) Explain the procedure to measure interconnect delay. (8)
