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Question Paper Code : 91510

M.E. DEGREE EXAMINATION, JANUARY 2012.

First Semester

Applied Electronics

AP 9212 — ADVANCED DIGITAL SYSTEM DESIGN

(Common to M.E. VLSI Design)

(Regulation 2009)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Differentiate between state table and excitation table.

2. Draw ASM diagram for a serial adder.

3. What is a merger graph? Give example?

4. Differentiate between dynamic and static hazard.

5. State the conditions for faults to be equivalent and for faults to be redundant.

6. What is the significance of using BIST in Digital circuits?

7. Implement F = ABC' + AB'D'C + A'D using a PLA.

8. What is Programmable Interconnect Point?

9. What is Blocking and Non — blocking statement in VHDL?

10. What is a package?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Design a Moore type sequence detector to detect a serial input sequence of 1010.   (8)

    (ii) Design a mod 5 counter. Use JK flip-Flops.   (8)

Or

(b) The Message bits are encoded on a single line x, so as to synchronize with a clock. Bits are encoded so that 3 or more consecutive 1 's or 3 or more 0's should never appear on the input line x. An error indicating sequential circuit is to be designed to indicate an error by generating '1' on the output line z, coinciding with the third of every sequence of three zero's or three ones. Draw the state diagram for the error detector. Reduce the state diagram if possible and design the logic circuit using D Flip-flops. (16)

12. (a) Design a circuit with primary inputs A and B to give an output Z equal to 1 when A becomes 1 if B is already 1. Once Z = 1 it will remain so until A goes to 0. Draw the Timing diagram, the state diagram, primitive flow table for designing this circuit. (16)

Or

(b) Design a negative edge triggered T flip-Flop . The circuit has two inputs T and C and one output Q. The output state is complemented if T= 1 and the clock C changes from 1 to 0. Otherwise, under any other input conditions the output Q remains unchanged. (16)

13. (a) (i) What is a fault? Explain Boolean difference Method of Fault Diagnosis. (8)

(ii) Discuss compact algorithm. (8)

Or

(b) (i) Discuss the test generation by DFT scheme. (8)

(ii) Explain the path sensitization method. (8)

14. (a) (i) Give the PAL realization of the given function

ω (A, B, C,D, E, F) = Σm (0, 2, 6, 7, 8, 9, 12, 13)

x (A, B, C, D, E, F) = Σm (0, 2, 6, 7, 8, 9, 12, 13, 14)

y (A, B, C, D, E, F) = Σm (2, 3, 8, 9, 10, 12, 13)

z (A, B, C, D, E, F) = Σm (1, 3, 6, 9, 12, 4). (8)

(ii) Design a BCD to excess 3 code convertor and implement using suitable PLA. (8)

Or

(b) (i) Draw and explain the block diagram for XILINX FPGA. (8)

(ii) Implement the following Boolean functions using 3x 4 x 2 PLA

F_1 (a, b, c) = Σ (0, 1, 3, 4)

F_2 (a, b, c) = Σ (1, 2 3, 4, 5). (8)

15. (a) (i) Explain Behavioral modeling with a suitable example. (8)

(ii) Design a 8 bit parallel Adder using VHDL. (8)

Or

(b) (i) Design an ALU using VHDL. (10)

(ii) Write a test bench to test a 4 bit counter. (6)

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