Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 81052

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

First Semester

Applied Electronics

AP 9212/AP 912/UAP 9111 — ADVANCED DIGITAL SYSTEM DESIGN

(Common to M.E. VLSI Design, M.E. VLSI Design and Embedded Systems and M.E. Digital Electronics and Communication Engineering)

(Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the difference between the state graphs for Mealy and Moore machines?

2. State two reasons why a state table might be incompletely specified.

3. What is the most important consideration in making state assignments for asynchronous networks?

4. Define static and dynamic hazards.

5. What is the significance of Kohavi algorithm?

6. List out the different faults that may occur in combinational digital circuits.

7. List the advantages of PLD approach over a PAL approach.

8. List the general features of Xilinx FPGA.

9. State the advantage of HDL over traditional methods of digital design.

10. What are the requirements of behavioral modeling?

PART B — (5 × 16 = 80 marks)

11. (a) Design a sequential network to convert BCD to Excess-3 code. (16)

Or

(b) (i) Construct an SM chart for the control network of a binary divider. (8)

(ii) Write notes on the ASM realization using PLAs. (8)

12. (a) Illustrate the analysis of an asynchronous sequential network with S-R flip flops. (16)

Or

(b) Illustrate the design of an edge-triggered clocked T flip flop and find a primitive flow table with a minimum number of rows. (16)

13. (a) (i) With an example, illustrate the concept of path sensitizing in the detection of faults in digital circuits. (8)

(ii) With an example, explain how test generation can be achieved in testing a PLA. (8)

Or

(b) (i) Explain about various types of faults that may occur in PLAs. (8)

(ii) Discuss the Built in self test scheme used in digital circuits. (8)

14. (a) (i) With an example, explain how a logic function can be realized using FPGA. (8)

(ii) Explain how Xilinx FPGA can be reprogrammed. (8)

Or

(b) Explain the block schematic and architecture of Xilinx 2000 FPGA. (16)

15. (a) (i) Write a VHDL source code for JK flipflop. (8)

(ii) Write a VHDL source code for n-bit counter. (8)

Or

(b) Write a detailed note on necessity and types of test benches in the stimulation of VHDL code. (16)

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