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Question Paper Code : 81031

M.E. DEGREE EXAMINATION, JUNE 2012.

First Semester

Applied Electronics

AP 9212/248102/AP 912/10244 AE 103 — ADVANCED DIGITAL SYSTEM DESIGN

(Common to M.E. VLSI Design)

(Regulation 2009)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1.   Bring out the difference between Mealy model and Moore model.

2.   What is meant by redundant state?

3.   Define essential hazard.

4.   What is a primitive flow table?

5.   Differentiate static redundancy and dynamic redundancy.

6.   What is meant by a self testing circuit?

7.   Bring out the difference PLA and PAL.

8.   Compare FPGA with Programmable logic devices.

9.   List out some of the multiplying operators in VHDL.

10. Define structural modeling with an example.

PART B — (5 × 16 = 80 marks)

11. (a) A sequential network has one input (X) and two outputs (Y and Z). An output Y = 1 occurs every time the input sequence 010 is completed provided that the sequence 100 has never occurred. An output Z = 1 occurs every time the input 100 is completed. Note that once a Z = 1 output has occurred, Y = 1 can never occur, but not vice versa. Find a Mealy state graph and state table. Assume minimum number of states is 8. (16)

Or

(b) An iterative network has an output of 1 from the last cell if the input pattern 1011 or 1101 has occurred as inputs to any 4 adjacent cells in the network.

(i) Find a Moore state graph or table with a minimum number of states.

(ii) Make a suitable state assignment and derive one of the equation for a typical cell.

(iii) Derive the output equation. (16)

12. (a) A sequential network has two inputs (X_1 X_2) and one: output (Z). If the input sequence 00,01,11 occurs, Z becomes 1 and remains 1 until the input sequence 11,01,00 occurs. In this case Z becomes 0 and remains 0 until the first sequence occurs again. (Note that the last input in one sequence may be the first input in the other sequence).

(i) Find the minimum row flow table.

(ii) Make a proper state assignment and realize the flow table with SR flipflops and gates. (16)

Or

(b) A control mechanism for a vending machine accepts nickels and dimes. It dispenses merchandise when 20 cents is deposited; it does not give change if 25 cents is deposited. Design the FSM that implements the required control, using as few states as possible. Find a suitable state assignment and derive the next state and output expressions. (16)

13. (a) (i) Draw and explain about the generic built in self test scheme. (6)

(ii) Explain the self test circuit for RAM and the self test circuit for RAM with signature register with a neat diagram. (10)

Or

(b) Briefly explain the basic concept of D-algorithm. Determine the primitive d-cubes of fault (pdcfs) and the propagation d-cubes (pdcs) for the logic diagram shown in Figure 1. (16)
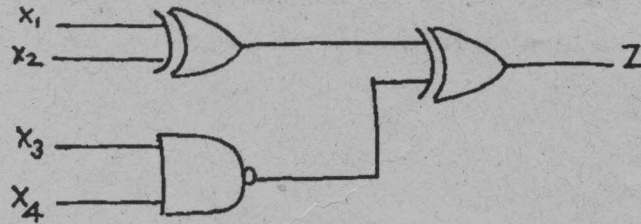

Figure 1

14. (a) Design a sequential network to multiply an 8-4-2-1 binary coded decimal digit by 3 to give a 5-bit binary number. For example, if the input is 0111, the output should be 10101. The input and output to the network should be serial with the least significant bit first. Assume that the input will be 0 at the fifth clock time and reset the network after the fifth output bit. Derive a state table with a minimum number of states (3 states) and design a network using a PLA and D flip flops and also draw the PLA table. (16)

Or

(b) With a neat block diagram, explain the XC4000 configurable logic block. (16)

15. (a) Write a VHDL module that describes one bit of a full adder with accumulator. The module should have two control inputs, Ad and L. If Ad = 1, the Y input (and carry input) are added to the accumulator. If L = 1, the input is loaded into the accumulator. (16)

Or

(b) An inhibited toggle flip flop has inputs I0, I1, T and reset and outputs Q and QN. Reset is active high and overrides the action of the other inputs. The flipflop works as follows : If I0 =1, the flip flop changes state on the rising edge of T; if I1 =1, the flip flop changes state on the falling edge of T.I0 = I1 = 0, no state changes(except on reset). Assume the propagation delay from T to output is 8 ns and from reset to output is 5 ns.

(i) Write a complete VHDL description of this flip flop.

(ii) Write a sequence of simulator commands that will test the flip flop for the input sequence I1 = 1, toggle T twice, I1 = 0, I0 = 1, toggle T twice. (16)

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