Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 71024

M.E. DEGREE EXAMINATION, JUNE/JULY 2013.

First Semester

Applied Electronics

AP 9212/AP 912/UAP 9111 — ADVANCED DIGITAL SYSTEM DESIGN

(Common to M.E. VLSI Design, M.E. VLSI Design and Embedded Systems and M.E. Digital Electronics and Communication Engineering)

(Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the practical applications of state diagram and state table.

2. Define the Moore state machine with a simple example.

3. Write a short note on data synchronizers.

4. What is meant by races?

5. Define the term fault diagnosis.

6. List the various testability algorithms.

7. Give the differences between CPLD and FPGA.

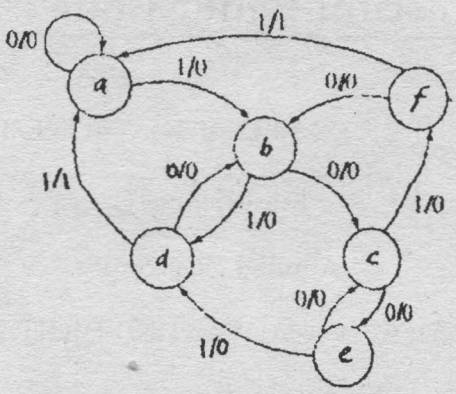
8. How synchronous design differs from asynchronous design?

9. Give the comparison between structural and switch level modeling.

10. What are test benches?

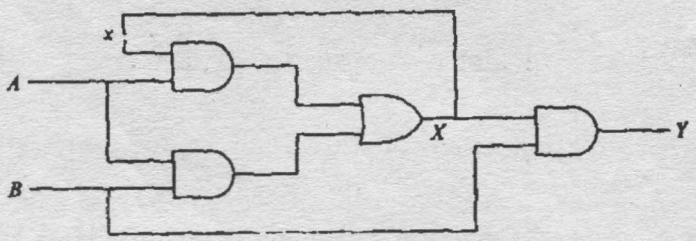
PART B — (5 × 16 = 80 marks)

11. (a) Reduce the following Mealy model state transition diagram using row elimination method. (16)

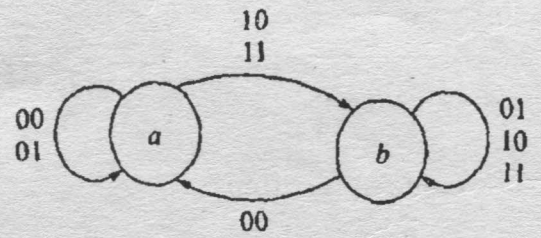


Or

(b) Analyze the Mealy model asynchronous sequential circuit of the following figure and show its stable state and corresponding outputs. Also give its state diagram. (16)



12. (a) (i) Design an asynchronous sequential logic circuit for state transition diagram shown in figure. (8)



(ii) Briefly explain about the design of vending machine controller. (8)

Or

(b) Describe in detail about the various types of hazards in the asynchronous sequential circuit. (16)

13. (a) Explain in detail about the following topics.

(i) Boolean difference method (8)

(ii) Path sensitization method. (8)

Or

(b) Explain in detail about the following topics.

(i) Fault in PLA (8)

(ii) Built in self test. (8)

14. (a) Discuss in detail about the Xilinx FPGAs. And explain about the structure of Xilinx 4000 family FPGA device. (16)

Or

(b) Realize a 4-bit parallel in parallel out shift register using PAL (or) PLA. (16)

15. (a) (i) Write a VHDL program for serial adder circuit. (8)

(ii) Write a VHDL program for 8:1 multiplex circuit. (8)

Or

(b) (i) Write a VHDL program for multiplier circuit. (8)

(ii) Write a VHDL program for 1:8 demultiplexer circuit. (8)

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