Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 11030

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

First Semester

Applied Electronics

AP 9212/AP 912/UAP 9111 — ADVANCED DIGITAL SYSTEM DESIGN

(Common to M.E. VLSI Design)

(Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Draw the block diagram of Moore model of a clocked synchronous sequential network.

2. What is transition period and stable period?

3. Define race-around condition.

4. What is data synchronizer?

5. List the assumptions about type of fault to be considered.

6. What are the DFT schemes?

7. Compare PLA and PAL.

8. List the advantages of Xlinx FPGA.

9. What are the guidelines to be followed while making state assignments?

10. Write VHDL code for a half adder.

PART B — (5 × 16 = 80 marks)

11. (a) For the clocked synchronous sequential network shown in Fig. 11 (a), construct the excitation table, transition table, state table and state diagram. (16)

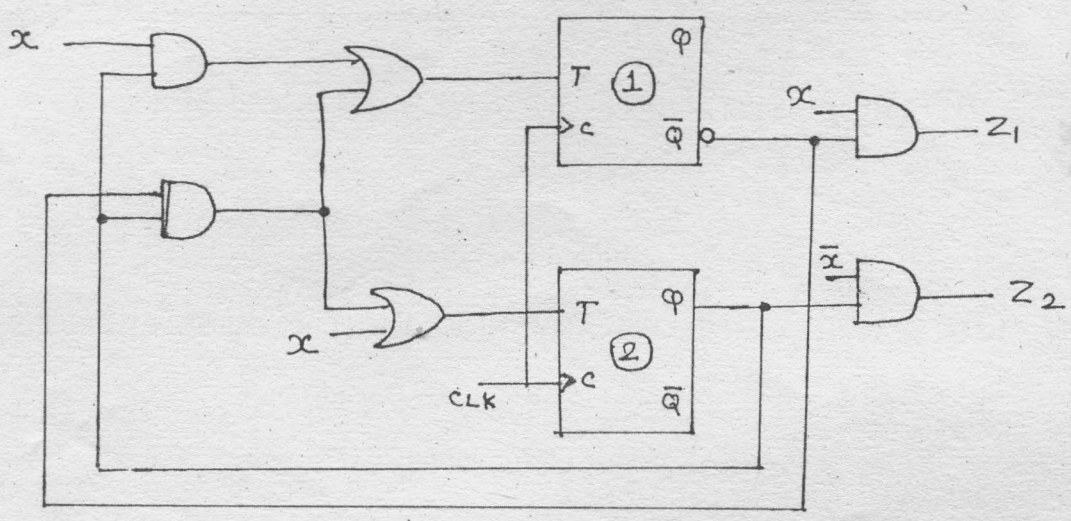

Fig. 11 (a)

Or

(b) (i) Construct an ASM block for a mod-8 binary up-down counter. (8)

(ii) Draw an ASM chart to design a control logic of a binary multiplier. Realize the same using MUX, decoder and D-type flip flops. (8)

12. (a) Obtain a primitive flow table and a minimal-row table for a fundamental mode asynchronous sequential network meeting the following requirements:

(i) There are two inputs X_1 and X_2 and a single output Z.

(ii) The inputs X_1 and X_2 never change simultaneously.

(iii) The output is to be 1 if X_1 was the last input variable to change value. On the other hand, the output is to be 0 if X_2 was the last input variable to change value. (16)

Or

(b) Explain static, dynamic and essential hazards with one example for each. (16)

13. (a) Using the path-sensitization method and Boolean difference method find the test vectors for SA0 fault on input line 1 and SA1 fault on the internal line 2 of the circuit shown in Fig.13 (a). (16)

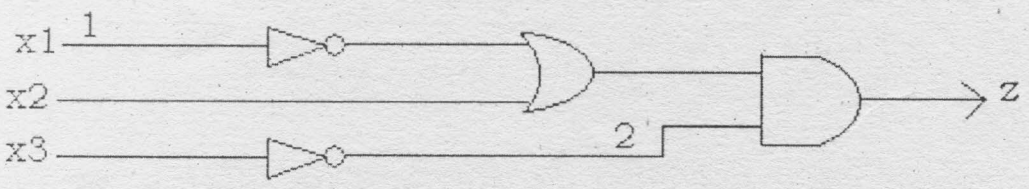

Fig.13 (a)

Or

(b) (i) Discuss the BIST scheme for PLD and CPLDs. (8)

(ii) Apply D-algorithm to detect '*h*', SA0 fault in Fig. 13 (b) (ii) and derive the test vectors. (8)

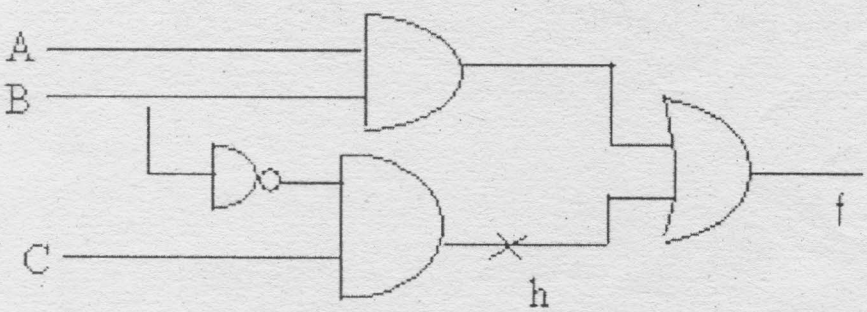

Fig. 13 (b) (ii)

14. (a) (i) Design a BCD-to-Excess 3 code converter using PLA circuit. (8)

(ii) Draw the general structure of an FPGA and explain how a logic-function can be realized on FPGA with a simple example. (8)

Or

(b) Design a four-way traffic light controller that will keep traffic moving efficiently along two busy streets that intersect. Implement the controller using PALs. (16)

15. (a) Explain the operators and packages of VHDL. (16)

Or

(b) Write VHDL program for 4-bit synchronous binary counter with its state table. (16)

———————