Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 83353

M.E. DEGREE EXAMINATION, JANUARY 2014.

Elective

VLSI Design

VL 7004 — ASYNCHRONOUS SYSTEM DESIGN

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Give the importance of Muller C-element in the asynchronous circuit design.
2. Explain pipelines and rings in a circuit with an example.
3. Define fork, join and merge.
4. Compare the performance analysis in synchronous and asynchronous circuits.
5. Differentiate hazards and faults in digital circuits.
6. Mention the data validity schemes used in bundled data protocols and circuits.
7. Expand VHDL and its significance in VLSI circuit design.
8. Compare VHDL and CSP type languages.
9. Give a general program structure for the BALSA language.
10. Mention the different channel registers available in DMA controller.

PART B — (5 × 16 = 80 marks)

11. (a) With the help of a neat diagrams explain the different circuit implementation styles of the handshake protocols. (16)

Or

(b) Explain in detail about the various building blocks of asynchronous circuits with suitable examples for the data flow structures. (16)

12. (a) Discuss in detail about the way of performance analysis and optimisation with the help of dependency graph. (16)

Or

(b) Explain the concept of mutual exclusion, arbitration and metastability with suitable example. (16)

13. (a) Discuss in detail about the advanced method of controlling latch circuits with proper example. (16)

Or

(b) Discuss in detail about the role of state holding elements in the design of speed independent control circuits. (16)

14. (a) Explain the concept of concurrency and message passing in CSP language with examples. (16)

Or

(b) Explain in detail about the BALSA tool set and the design flow for the asynchronous system design. (16)

15. (a) Discuss in detail about the DMA controller structure and its BALSA description. (16)

Or

(b) Explain in detail about the BALSA shifter with necessary diagrams. (16)