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Question Paper Code : 14107

M.E. DEGREE EXAMINATION, JANUARY 2015.

Elective

VLSI Design

VL 7004 — ASYNCHRONOUS SYSTEM DESIGN

(Regulation 2013)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How the superfluous return to zero transitions present in 4 phase bundled data protocol is avoided?
2. Is the Muller circuit speed independent or not? Reason out.
3. Define reverse latency and dynamic wavelength.
4. Draw the data dependency graph for a 3-stage pipeline.
5. What is min-max delay and unbounded delay?
6. What is pull channel and biput channel?
7. State the key characteristics of CSP.
8. Write a tangram program for a 2-place shift register.
9. How area minimisation can be done in Balsa language?
10. How Balsa supports recursive definitions? Give an example.

PART B — (5 × 16 = 80 marks)

11. (a) Discuss briefly about circuit implementation styles.

Or

- (b) Explain the different static dataflow circuits used in the design of asynchronous circuit with suitable examples.

12. (a) Analyse the performance of shift register with parallel load and discuss the implementation fork, join and merge.

Or

- (b) (i) Discuss the implementation of 3-stage pipeline using ring. (8)
(ii) Explain the terms mutual exclusion, arbitration and probability of meta stability. (8)
13. (a) Explain the synthesis procedure used for C-element and use of petrify for a control circuit for the 4-phase bundled data implementation of the latch.

Or

- (b) Implement a circuit with choice using state-holding gates and write briefly about data validation schemes for 2 phase and 4 phase bundled data.
14. (a) (i) Write a Tangram program for GCD and 2 place ripple. (4)
(ii) Write a brief note on tool set, design flow of Balsa with suitable examples. (12)

Or

- (b) Explain about Tangram syntax directed compilation and auxillary Balsa tools.
15. (a) Write a Balsa code for up/down counter and an arbiter tree.

Or

- (b) Give a detailed description of DMA controller.