Reg. No. | | | | | | | | | | | | |

Question Paper Code : 66319

M.E. DEGREE EXAMINATION, DECEMBER 2015/JANUARY 2016

Elective

VLSI Design

VL7004 – ASYNCHRONOUS SYSTEM DESIGN

(Regulations : 2013)

Time : 3 Hours] **[Max. Marks : 100**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Define the term 4-phase protocol.
2. Define the term bubbles and tokens with an example.
3. Write down the three parameters used to characterize performance of an asynchronous pipeline.
4. Draw the following components :

   (i) Fork (ii) Join (iii) Merge
5. What is a Petri net ?
6. Differentiate Push channel and Pull channel.
7. What is CSP ? Write its key characteristics.
8. What is Balsa ? Write its key advantage.
9. Name the four global registers.
10. List the functions of three name spaces in Balsa.

PART – B (5 × 13 = 65 Marks)

11. (a) Draw and explain the structure of Muller pipeline.

OR

(b) Explain the Building blocks of static data-flow structures.

12. (a) Explain Latency, Throughput and Dynamic wavelength.

OR

(b) Write short notes on Mutual exclusion, arbitration and metastability.

13. (a) Define STG and explain its characteristics.

OR

(b) Explain "Advanced latch control circuits" in 4-phase bundled-data latch control circuits.

14. (a) Explain Balsa tool sets.

OR

(b) Describe Martin's translation process.

15. (a) Write short note on data types in Balsa.

OR

(b) Explain DMA controller structure.

PART – C (1 × 15 = 15 Marks)

16. (a) Write a Tangram program for a 2-place shift register and a 2-place ripple FIFO.

OR

(b) Design a control circuit for a 4-phase bundled-data latch using petrify.

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