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Question Paper Code : 63061

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Elective

Applied Electronics

AP 7008 — DSP INTEGRATED CIRCUITS

(Common to M.E. Medical Electronics and M.E. VLSI Design)

(Regulation 2013)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1.   What are the features of application specific IC'S for DSP?

2.   What is the propagation delay of CMOS inverter?

3.   What is the significance of sampling frequency in digitization of analog signals?

4.   List out the applications of adaptive DSP algorithms.

5.   Give examples for FIR chips.

6.   Determine signal to noise ration of safely scale 16-point FET.

7.   Mention the purpose of using complex PE$_s$ in DSP.

8.   Distinguish multiprocessor and DSP architectures.

9.   List the applications of Cordic algorithm.

10. State the factors that influence the memory size in DSP processors.

PART B — (5 × 16 = 80 marks)

11. (a) Explain different types of partitioning techniques. (16)

Or

(b) (i) Compare CMOS and bipolar technology. (8)

(ii) Design a half subtractor with CMOS technology. (8)

12. (a) (i) An 8 point Sequence is given by $x\ (n)$ = (1, 1, 1, 1, 2, 2, 2, 2). Compute 8 point DFT of x (n) by radix-2 DIT-FFT. (10)

(ii) Discuss the computations involved in DFT and FFT. (6)

Or

(b) Explain in detail about the Image coding with an example. (16)

13. (a) For Analog T.F of Ha (s) = $\dfrac{s+2}{s^2 + 2s + 10}$ determine H (z) by

(i) Impulse invariant transformation

(ii) Bilinear transformation.

Or

(b) Explain the procedure to obtain the product quantization noise model of Second order IIR system. (16)

14. (a) (i) Compare and contrast standard DSP architecture with ideal DSP architecture. (8)

(ii) Discuss the operation of systolic front arrays with neat diagram. (8)

Or

(b) Write the steps involved in mapping DSP algorithm to hardware. (16)

15. (a) (i) Explain the steps involved in the addition of 25_{10} and 65_{10} using CSD representation. (6)

(ii) Explain the implementation of 8 × 8 Wallace Tree multiplier. (10)

Or

(b) (i) What is DCT Processor? Explain its algorithm which is followed in the processor. (8)

(ii) Design an improved shift accumulator system with neat diagram. (8)

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