Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 91847

M.E. DEGREE EXAMINATION, JANUARY 2012.

First Semester

VLSI Design

VL 9211 – DSP INTEGRATED CIRCUITS

(Common to M.E. Applied Electronics)

(Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is CMOS Logic?
2. What are the process Technology for VLSI?
3. State sampling theorem.
4. Draw the basic Butterfly diagram for DIT algorithm.
5. Draw the structure for the following difference equation

   $Y(n)=x(n)+0.5\times(n-1)+0.75\times(n-2)$.
6. Define first order coefficient sensitivity.
7. What is the advantage of shared memory architecture?
8. What are the advantages of Bit serial architecture?
9. What is redundant number system?
10. Name any Two FFT processor.

PART B — (5 × 16 = 80 marks)

11. (a) Explain in detail DSP system design.

Or

(b) (i) Draw CMOS NAND gate circuit and explain the working principle. (4)

(ii) Write a note on VLSI Technology. (12)

12. (a) Draw the 8-point decimation infrequency flow chart for the computation of DFT coefficients (the radix-2 algorithm).

Or

(b) (i) Describe an Adaptive DSP system using an example. (8)

(ii) Explain any one application of discrete cosine transform in image compression. (8)

13. (a) (i) Discuss the procedure for designing IIR filters from analog filters. (8)

(ii) Write a note on multirate system. (8)

Or

(b) (i) Explain finite word length effects in IIR filter by taking an example. (8)

(ii) Explain about scaling and round-off noise. (8)

14. (a) (i) Describe the procedure for converting DSP algorithm into DSP hardware.

(ii) Explain about "Systolic and wave front arrays". (8)

Or

(b) (i) What are the characteristics of ideal DSP architecture? Discuss.

(ii) What is PE? Explain bit serial PE in detail.

15. (a) Write short notes on:

(i) Residue number system and its relevance to DSP system. (8)

(ii) Explain the layout of VLSI circuit for DCT processor. (8)

Or

(b) Explain in detail about CORDIC algorithm and Bit Parallel arithmetic circuits.
