Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 83021

M.E. DEGREE EXAMINATION, JANUARY 2014.

Elective

VLSI Design

AP 7008 — DSP INTEGRATED CIRCUITS

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the features of Application Specific IC of DSP.

2. What is the effect of temperature on propagation delay of IC?

3. List any two commercial DCT Processor integrated circuits.

4. What are functional blocks of Transform coding system used in image coding?

5. List any two FIR filter chips.

6. Draw the spectrum of the signal $x(t) = \cos\omega t$, which is up-sampled by a factor 4.

7. Differentiate multi-processors and multi-computers.

8. What are the different types of interconnection topologies?

9. Convert the number 0.0110100101_2 in 2's complement representation to CSDC representation.

10. Mention any four adders using Bit-Parallel arithmetic.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain different facets of DSP system briefly. (8)

(ii) Discuss briefly about the partitioning techniques in system design. (8)

Or

(b) Implement sum output of half adder, using Ratioed logic, CMOS logic and Precharge-evaluation logic with minimum number of transistors.(16)

12. (a) Explain any one type of adaptive filter and discuss the applications of adaptive filters. (16)

Or

(b) Draw and explain the butterfly architecture for eight-point DCT. (16)

13. (a) Explain and design a FIR filter using Parks Mcclellan and Rabiner algorithm for an interpolator, which interpolates the sampling frequency by 4, Pass-band ripple <0.6dB and stop band attenuation of minimum 65dB. (16)

Or

(b) (i) Explain briefly about safe scaling. (8)

(ii) Write short notes on error spectrum shaping . (8)

14. (a) Explain the architecture of a Motorola DSP processor with its block diagram. (16)

Or

(b) Write short notes on Systolic and Wavefront arrays processors. (16)

15. (a) (i) Explain the architecture of any one type of multiplier with its block diagram. (8)

(ii) Explain the architecture of basic shift accumulator. (8)

Or

(b) Explain the specification and system design phase of FFT processor. (16)

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