Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 13038

M.E. DEGREE EXAMINATION, JANUARY 2015.

Elective

Applied Electronics

AP 7008 — DSP INTEGRATED CIRCUITS

(Common to M.E. VLSI Design and M.E. Medical Electronics)

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the design steps involved in direct mapping technique?
2. Design carry output of half adder using nMOS logic?
3. Draw the spectrum of signal $x(t) = \cos \omega t$, sampled by frequency 5ω.
4. Write MSDCT pair.
5. Mention any two commercial FIR Chips.
6. What is meant by safe scaling?
7. What are the features of standard DSP architecture?
8. What is the type of communication protocol between PEs of systolic and wavefront array?
9. Perform addition of 14_{10} and 20_{10} using RNS with modules (7,3,2).
10. What are the constraints of placement?

PART B — (5 × 16 = 80 marks)

11. (a) Explain different approaches used in partitioning DSP system design.

Or

(b) Implement the expression $Z = ((A' + B')' + CD)'$ using ratioed logic, CMOS logic and precharge evaluation logic.

12. (a) (i) Explain the use of signal flow graph with an example. (8)

(ii) Discuss about the various filter structures. (8)

Or

(b) (i) Find the EDCT of the sequence $x(n)=\{1,1,0,0,0,1,1,1\}$ using matrix method. (10)

(ii) Explain the principle of any one Adaptive DSP algorithm. (6)

13. (a) (i) Design FIR filter using Parks, McClellan and Rabiner algorithm to interpolate sampling frequency by 3, input signal is band limited to 0 to $\pi/4$, pass band ripple <0.5dB and stop band attenuation of minimum 60dB. (8)

(ii) Discuss about multirate systems. (8)

Or

(b) (i) Show that coefficient sensitivity depends on the scaling criteria used in a system. (8)

(ii) Explain briefly about parasitic oscillations in the output of a system. (8)

14. (a) Explain the architecture of any DSP processor with its internal block diagram.

Or

(b) (i) What are the methods to eliminate the memory bandwidth bottleneck in the shared memory architecture? Explain. (8)

(ii) Explain the operation of Bit-serial PEs. (8)

15. (a) Briefly explain about Bough-Wooley multiplier and Basic shift accumulator.

Or

(b) (i) Explain Lee-Mores algorithm with an example. (10)

(ii) Write about the Layout of VLSI circuits. (6)
