Reg. No. | | | | | | | | | | | | |

Question Paper Code : 66019

M.E. DEGREE EXAMINATION, DECEMBER 2015/JANUARY 2016

Elective

Applied Electronics

AP7008 : DSP Integrated Circuits

(Common to M.E. Medical Electronics and M.E. VLSI Design)

(Regulations : 2013)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. What is meant by Edge-in Approach of Partitioning Technique ?
2. What is the effect of propagation delay in ICs ?
3. Draw the spectrum of signal $x(t) = \cos\omega t$ sampled by the sampling frequency $f_s = 5\omega/2$.
4. What are the applications of adaptive DSP algorithms ?
5. What are the features of half band FIR filter ?
6. What is the use of Error Spectrum Shaping ?.
7. What are the functional modules of DSP system architectures ?
8. Draw the structure of wave front array.
9. Convert the decimal number 48.5_{10} into CSDC.
10. Find the number of AND operations required for multiplication of two n-bit numbers using Shift and Add multiplication.

PART – B (5 × 13 = 65 Marks)

11. (a) Explain different Facets of DSP System Design.

OR

(b) Implement carry output of Full adder using CMOS and Precharge-Evaluation logic.

12. (a) Draw and explain the block diagram of RLS lattice filter for N = 4.

OR

(b) Design an architecture to find 8 point DCT with minimum number of arithmetic operations.

13. (a) Suggest a system for interpolation of sample frequency by a factor 3.5. Determine the cutoff and stop-band edges of the filters involved.

OR

(b) Show that coefficient sensitivity depends on the scaling criteria used.

14. (a) Explain the architecture of DSP with reference to pipelining stages and CPU features.

OR

(b) Explain any two methods to reduce memory access of shared memory architecture.

15. (a) Derive the logic realization of partial products of 4 × 4 Baugh Wooley Multiplier.

OR

(b) Briefly explain about Slicing floor-plan and Global routing.

PART – C (1 × 15 = 15 Marks)

16. (a) Explain the specification and system design phase of FFT processor.

OR

(b) Discuss the various hierarchical levels in the design of DCT processor.
