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**Question Paper Code : 11912**

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

First Semester

VLSI Design

VL 9211/ VL 911/ 10244 VLE 13 — DSP INTEGRATED CIRCUITS

(Common to M.E. Applied Electronics and M.E. Medical Electronics)

(Regulation 2009 / 2010)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the effect of temperature on the propagation delay of IC?
2. What are the features of application specific signal processors?
3. Mention few applications using adaptive DSP algorithms.
4. Determine the transfer function of a system that is described by the difference equation.  $y(n) = b y(n-1) + a x(n)$ .
5. Show that for symmetric impulse response change in phase is linearly proportional to frequency.
6. What do you mean by parasitic oscillations?
7. What is the aim of using complex PEs in DSP?
8. Compare multiprocessor with multi computer in the contest of DSP systems.
9. What are the disadvantages of Bit-serial arithmetic in DSP system?
10. State the steps in the layout of VLSI integrated circuits.

PART B — (5 × 16 = 80 marks)

11. (a) What is the importance of partitioning in any circuit design? Discuss different types of partitioning in detail. (16)

Or

- (b) (i) Define propagation delay in CMOS circuits. Derive the expression for charge time and discharge time. (10)
- (ii) Estimate the propagation delay for a CMOS inverter that is loaded with five identical inverters connected in parallel. The wiring corresponds to a load of about 5 fF. Use the following values :

$$\mu_n = 4.62 \times 10^{-2} \text{ m}^2/\text{Vs}, \mu_p = 1.6 \times 10^{-2} \text{ m}^2/\text{Vs}, T_{ox} = 155 \text{ \AA}$$

$$W_{ndrawn} 2.0 \mu\text{m}, W_{neff} = 0.84 \mu\text{m}, L_{ndrawn} = 0.8 \mu\text{m}, L_{neff} = 0.8 \mu\text{m}$$

$$W_{pdrawn} 20 \mu\text{m}, W_{peff} 1.34 \mu\text{m}, L_{pdrawn} = 0.8 \mu\text{m}, L_{peff} = 0.96 \mu\text{m}$$

$$V_{Tn} = 0.84 \text{ V}, V_{Tp} = -0.73 \text{ V} \text{ and } V_{DD} = 5 \text{ V.} \quad (6)$$

12. (a) (i) Find the magnitude and phase of first order system,  $H(z)$ , at  $\omega = \pi/3$  rad and  $\omega = \pi/4$  rad  $H(z) = \frac{z+1}{z-0.5}$ .
- (ii) Find the T.F. for the structure shown in Fig. 1.

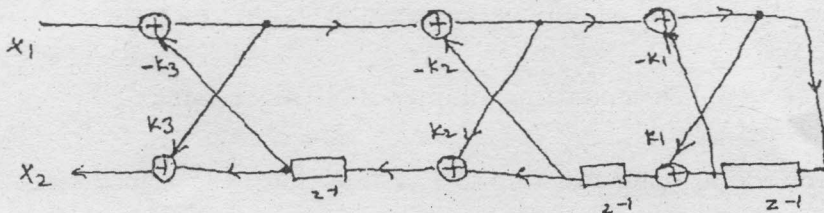


Fig.1

Or

- (b) (i) Find the DFT of the sequence.

$$x(n) = 1, n = 0, 1, 2, 3$$

$$= 0, n = 4, 5, 6, 7$$

and hence find  $|X(i)|$ .

- (ii) Draw the flow chart of decimation in time (DIT) algorithm of FFT. Assume  $N = 8$ .

13. (a) (i) Determine the relation between the group delays of an analog filter and the corresponding digital filter that is obtained by bilinear transformation. (8)
- (ii) Design an interpolates that increases the sampling frequency with a factor two, from 1.6 MHz to 3.2 MHz. The energy of the input signal is contained within the band 0 to 680 kHz. No signal is noises present above this band. The input data word length is 12 bits and output signal should have essentially the same accuracy. (8)

Or

- (b) (i) Show that a two-port adaptor is pseduo-loss less. (8)
- (ii) Show that the quantization scheme will suppress parasitic oscillations. (8)
14. (a) Explain the distinguishing features of any one DSP processor with its internal block diagram.

Or

- (b) Briefly explain about the systolic and wavefront arrays.
15. (a) Describe the carry ripple and carry save array implementation styles in realizing bit parallel multipliers. (16)

Or

- (b) Draw the structure of a hardware butterfly processor for implementation of FFT algorithm and explain the individual computational elements. (16)
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