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Question Paper Code : 91849

M.E. DEGREE EXAMINATION, JANUARY 2012.

First Semester

VLSI Design

VL 9213 — SOLID STATE DEVICE MODELING AND SIMULATION

(Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw the equivalent Circuit of MOS transistor.
2. Suppose the MOSFET Configuration is to be used as a capacitor. If the width and length of the MOSFET are both 100 micrometer. Estimate the capacitance.
3. What are the noise sources in MOSFET?
4. Give a brief note on thermal noise modeling.
5. What are the limitations of modeling the MOSFET?
6. What is parasitics model?
7. List the effects of drain current in EKV model.
8. Write a note on MOS model 9.
9. What is quality assurance?
10. How is device mismatch modelled for RF application?

PART B — (5 × 16 = 80 marks)

11. (a) Describe high frequency behavior of MOS transistor with necessary diagram. (16)

Or

(b) Explain in detail the parasitic modelling of resistors and capacitors. (16)

12. (a) With neat sketch, explain the modeling of Non Linearity in CMOS devices. (16)

Or

(b) Explain flicker and thermal noise modeling. (16)

13. (a) (i) What is mobility model? Explain its working. (8)

(ii) Discuss the modeling of junction diode model using BSIM4 MOSFET. (8)

Or

(b) Draw the sketch of gate tunnelling current model and substrate current model and explain. (16)

14. (a) Explain the modeling of charge storage effects and non-quasi-static model. (16)

Or

(b) With neat sketch, explain the operation of EKV model. (16)

15. (a) Explain Benchmark circuits for quality assurance. (16)

Or

(b) Describe the modeling of device mismatch for analog/RF applications. (16)