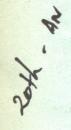
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Maximum: 100 marks



## Question Paper Code: 71870

M.E. DEGREE EXAMINATION, JUNE/JULY 2013.

First Semester

VLSI Design

VL 9213/VL 913/10244 VL 105 – SOLID STATE DEVICE MODELLING AND SIMULATION

(Regulation 2009/2010)

Time: Three hours

Answer ALL questions.

PART A —  $(10 \times 2 = 20 \text{ marks})$ 

- 1. Draw the equivalent circuit of MOS capacitor and define each element.
- 2. What are the issues involved in developing MOSFET model for RF applications?
- 3. What is DIBL effect?
- 4. List the non ideal effects of MOS.
- 5. Define inversion layer quantisation.
- 6. Differentiate between metal and poly resistor.
- 7. Give any four attractive features of EKV model.
- 8. State the effect of reverse short channel on MOS transistor performance.
- 9. What is physical model?
- 10. Name any two benchmark circuits.

PART B —  $(5 \times 16 = 80 \text{ marks})$ 

11. (a) Discuss the equivalent circuit of MOSFET for RF applications and explain how HF model parameters are extracted.

Or

(b) Explain the modelling of parasitic BJT, Resistors and capaciters using various methods.

|     |     | (ii) Draw the small signal schematic of noise sources and discuss he they are calculated analytically.   | (8)       |
|-----|-----|--|-----------|
| 13. | (a) | Elaborate on the various options for modelling gate electrode resistant in MOSFET. Draw the schematic.   | cé        |
|     |     | Or   |           |
|     | (b) | Explain:   |           |
|     |     |  | (8)       |
|     |     | (ii) Layout – dependent parasitics model.  | (8)       |
| 14. | (a) | How is velocity saturation and channel length modulation taken in account in EKV model? Explain.   | to        |
|     |     | Or   |           |
|     | (b) | (i) Depending on layout difference, how are parasitics modelled BSIM4?   | in<br>(6) |
|     |     | (ii) Describe the MOSAI model. (1  | .0)       |
| 15. | (a) | What is a physical model? Explain the modeling of device mismatch Resistor, MOS transistor for RF applications.  | in        |
|     |     | Or continue to the second seco |           |
|     | (b) | Discuss the test automation of CMOS RF circuits.   |           |
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Define the various non linearities in CMOS devices and modelling using

(i) What are the various sources of distortion in analog CMOS circuits?

Or

12.

(a)

(b)

any one method for each.