Reg. No. | | | | | | | | | | | | |

Question Paper Code : 83354

M.E. DEGREE EXAMINATION, JANUARY 2014.

First Semester

VLSI Design

VL 7101 – VLSI SIGNAL PROCESSING

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List-out the various applications of digital signal processing.

2. Give the comparison table between FPGA and digital signal processors.

3. What are the two steps in the unfolding algorithm?

4. Define the term fine-grain pipelining.

5. Write a short note on cyclic convolution.

6. Derive 2-parallel fast FIR filter structure.

7. Write a short note on hybrid radix-4 addition.

8. Define the term scaling.

9. List out the five steps in interactive matching process for multiple constant multiplication under numerical strength reduction.

10. What is meant by clock skew?

PART B — (5 × 16 = 80 marks)

11. (a) Explain in detail about the various technologies in FPGA. (16)

Or

(b) Explain the following terms in VLSI design implementation.

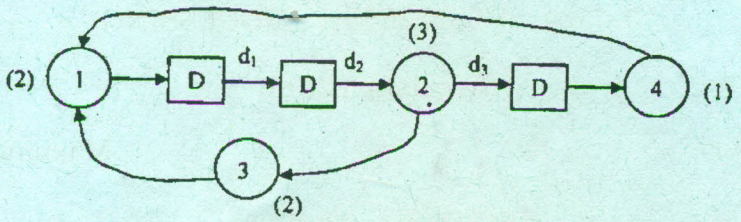
(i) Logic synthesis. (4)

(ii) Logic partitioning. (4)

(iii) Logic fitting. (4)

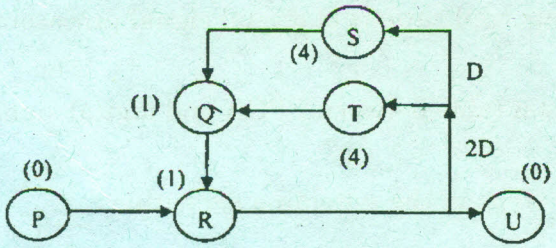
(iv) Timing extraction. (4)

12. (a) Compute the iteration bound for the following DFG. (16)



Or

(b) Obtain the 2-unfold structure for the following figure. (16)



13. (a) Construct a 2 × 2 convolution algorithm using modified Cook-Toom algorithm for $\beta_0 = 0, \beta_1 = 1$ and compare the number of multiplications and additions with direct implementation. (16)

Or

(b) Design a 4-parallel rank-order filter with substructure sharing for a window size = 7. Use only 1 × l, 2 × 2, 2 × 4 and 6 × 1 blocks. (16)

14. (a) Explain in detail about the following topics.

(i) Derivation of one-multiplier Lattice filter (8)

(ii) Derivation of scaled-normalized Lattice filter (8)

Or

(b) Obtain CSD number for 0.10011100010111 and use Horner's rule to get a structure. (16)

15. (a) Derive an expression for clock period in wave pipelining. (16)

Or

(b) Explain in detail about the pipeline concepts used in sequential circuits. (16)
